

# Single-Channel, 12- and 16-Bit Programmable Current Output and Voltage Output Digital-to-Analog Converters for 4-mA to 20-mA Current Loop Applications

Check for Samples: [DAC7760](#), [DAC8760](#)

## FEATURES

- **Current Output:** 4 mA to 20 mA;  
0 mA to 20 mA; 0 mA to 24 mA
- **Voltage Output:**
  - 0 V to 5 V; 0 V to 10 V;  $\pm 5$  V;  $\pm 10$  V
  - 0 V to 5.5 V; 0 V to 11 V;  $\pm 5.5$  V;  $\pm 11$  V (10% Overrange)
- $\pm 0.1\%$  FSR Total Unadjusted Error (TUE) Max
- DNL:  $\pm 1$  LSB Max
- Simultaneous Voltage and Current Output
- Internal 5-V Reference (10 ppm/ $^{\circ}$ C, max)
- Internal 4.6-V Power-Supply Output
- Reliability Features:
  - CRC Check and Watchdog Timer
  - Thermal Alarm
  - Open Alarm, Short Current Limit
- Wide Temperature Range:  $-40^{\circ}$ C to  $+125^{\circ}$ C
- 6-mm  $\times$  6-mm QFN-40; TSSOP-24 Packages

## APPLICATIONS

- 4-mA to 20-mA Current Loops
- Analog Output Modules
- Building Automation
- Environment Monitoring
- Programmable Logic Controllers (PLCs)
- Field Sensors and Process Transmitters

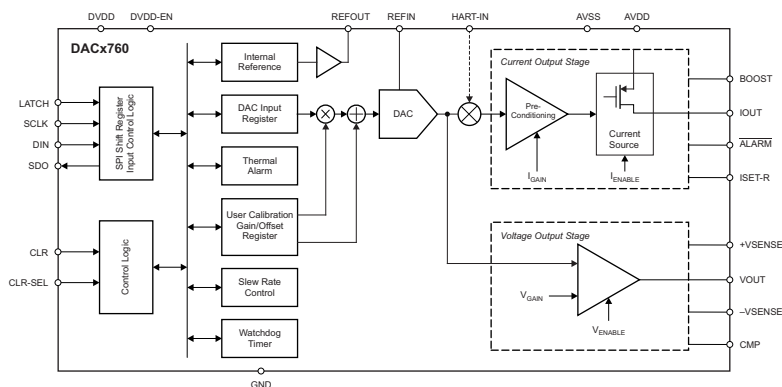
## DESCRIPTION

The [DAC7760](#) and [DAC8760](#) are low-cost, precision, fully-integrated, 12-bit and 16-bit digital-to-analog converters (DACs) designed to meet the requirements of industrial process-control applications. These devices can be programmed as a current output with a range of 4 mA to 20 mA, 0 mA to 20 mA, or 0 mA to 24 mA; or as a voltage output with a range of 0 V to 5 V, 0 V to 10 V,  $\pm 5$  V, or  $\pm 10$  V, with a 10% overrange (0 V to 5.5 V, 0 V to 11 V,  $\pm 5.5$  V, or  $\pm 11$  V). Both current and voltage outputs can be simultaneously enabled while being controlled by a single data register.

These devices include a power-on-reset function to ensure powering up in a known state (both IOU<sub>T</sub> and VO<sub>U</sub><sub>T</sub> are disabled and in a Hi-Z state). The CLR and CLR-SEL pins set the voltage outputs to zero-scale or midscale, and the current output to the low end of the range, if the output is enabled. Zero and gain registers can be programmed to digitally calibrate the device in the end system. The output slew rate is also programmable by register. These devices can superimpose an external HART<sup>®</sup> signal on the current output and can operate with either a single +10-V to +36-V supply, or dual supplies of up to  $\pm 18$  V. All versions are available in both 6-mm  $\times$  6-mm QFN-40 and TSSOP-24 packages.

## RELATED DEVICES

RESOLUTION (BITS)	CURRENT AND VOLTAGE OUTPUT	CURRENT OUTPUT
12	<a href="#">DAC7760</a>	<a href="#">DAC7750</a>
16	<a href="#">DAC8760</a>	<a href="#">DAC8750</a>



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### PACKAGE/ORDERING INFORMATION<sup>(1)</sup>

PRODUCT	RESOLUTION	TUE (%FSR)	DIFFERENTIAL NONLINEARITY (LSB)	SPECIFIED TEMPERATURE RANGE
DAC8760	16	0.2% (IOUT), 0.07% (VOUT)	±1	–40°C to +125°C
DAC7760	12	0.2% (IOUT), 0.07% (VOUT)	±1	–40°C to +125°C

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the device product folder at [www.ti.com](http://www.ti.com).

### ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted).<sup>(1)</sup>

	VALUE	UNIT
AVDD to AVSS	–0.3 to 40	V
AVDD to GND	–0.3 to 40	V
AVSS to GND	–20 to 0.3	V
DVDD to GND	–0.3 to 6	V
VOUT to AVSS	AVSS to AVDD	V
VOUT to GND <sup>(2)</sup>	AVSS to AVDD	V
IOUT to AVSS	AVSS to AVDD	V
IOUT to GND <sup>(2)</sup>	AVSS to AVDD	V
REFIN to GND	–0.3 to 6	V
REFOUT to GND	–0.3 to 6	V
Current into REFOUT	10	mA
Digital input voltage to GND	–0.3 to DVDD + 0.3	V
SDO to GND	–0.3 to DVDD + 0.3	V
ALARM to GND	–0.3 to 6	V
Operating temperature range	–40 to +125	°C
Storage temperature range	–65 to +150	°C
Junction temperature range (T <sub>J</sub> max)	+150	°C
Power dissipation	(T <sub>Jmax</sub> – T <sub>A</sub> )/θ <sub>JA</sub>	W
Electrostatic discharge (ESD) ratings	Human body model (HBM)	1500
	Charged device model (CDM)	1000

(1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

(2) AVSS tied to GND.

### THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>		DAC7760, DAC8760		UNITS
		RHA (QFN)	PWP (TSSOP)	
		40 PINS	24 PINS	
θ <sub>JA</sub>	Junction-to-ambient thermal resistance	32.9	32.3	°C/W
θ <sub>JCtop</sub>	Junction-to-case (top) thermal resistance	17.2	14.1	
θ <sub>JB</sub>	Junction-to-board thermal resistance	7.5	12.2	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.2	0.3	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	7.5	12.0	
θ <sub>JCbot</sub>	Junction-to-case (bottom) thermal resistance	1.4	0.63	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](http://www.ti.com/lit/zip/SRPA953).

## ELECTRICAL CHARACTERISTICS

At AVDD = +10 V to +36 V, AVSS = –18 V to 0 V, AVDD + |AVSS| ≤ 36 V, GND = 0 V, REFIN = +5-V external, and DVDD = +2.7 V to +5.5 V. For VOUT: R<sub>L</sub> = 1 kΩ, C<sub>L</sub> = 200 pF; for IOUT: R<sub>L</sub> = 300 Ω. All specifications are from –40°C to +125°C, unless otherwise noted. Typical specifications are at +25°C.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
<b>VOLTAGE OUTPUT</b>						
Voltage output ranges (normal mode)	AVDD ≥ 10 V	0		5	V	
	AVDD ≥ 10.5 V	0		10	V	
	AVSS ≤ –5.5 V, AVDD ≥ 10 V	–5		5	V	
	AVSS ≤ –10.5 V, AVDD ≥ 10.5 V	–10		10	V	
Voltage output range (overrange mode)	AVDD ≥ 10 V	0		5.5	V	
	AVDD ≥ 11.5 V	0		11	V	
	AVSS ≤ –6 V, AVDD ≥ 10 V	–5.5		5.5	V	
	AVSS ≤ –11.5 V, AVDD ≥ 11.5 V	–11		11	V	
Resolution	DAC8760	16			Bits	
	DAC7760	12			Bits	
<b>Accuracy<sup>(1)</sup></b>						
Total unadjusted error, TUE	T <sub>A</sub> = –40°C to +125°C	–0.07		+0.07	%FSR	
	T <sub>A</sub> = –40°C to +85°C	–0.06		+0.06	%FSR	
	T <sub>A</sub> = +25°C	–0.04	±0.015	+0.04	%FSR	
Differential nonlinearity, DNL	Monotonic			±1	LSB	
Relative accuracy, INL	T <sub>A</sub> = –40°C to +125°C			±0.040	%FSR	
	T <sub>A</sub> = –40°C to +85°C			±0.022	%FSR	
Bipolar zero error	T <sub>A</sub> = –40°C to +125°C	–7		+7	mV	
	T <sub>A</sub> = –40°C to +85°C	–6		+6	mV	
	T <sub>A</sub> = +25°C, ±5 V and ±5.5 V	–1.5	±0.5	+1.5	mV	
	T <sub>A</sub> = +25°C, ±10 V and ±11 V	–3	±1	+3	mV	
Bipolar zero error temperature coefficient			±1		ppm FSR/°C	
Zero-scale error <sup>(2)</sup>	Unipolar range (0-5 V, 0-5.5 V, 0-10 V, 0-11 V)	T <sub>A</sub> = –40°C to +125°C	–4		+4	mV
		T <sub>A</sub> = –40°C to +85°C	–2		+2	mV
		T <sub>A</sub> = +25°C	–0.6	±0.1	+0.6	mV
	Bipolar range (±5 V, ±5.5 V, ±10 V, ±11 V)	T <sub>A</sub> = –40°C to +125°C	–10		+10	mV
T <sub>A</sub> = +25°C		–3.5	±1	+3.5	mV	
Zero-scale error temperature coefficient			±2		ppm FSR/°C	
Offset error	T <sub>A</sub> = –40°C to +125°C, unipolar range	–4		+4	mV	
	T <sub>A</sub> = –40°C to +85°C, unipolar range	–2		+2	mV	
	T <sub>A</sub> = +25°C, unipolar range	–0.6	±0.1	+0.6	mV	
Offset error temperature coefficient			±1		ppm FSR/°C	
Gain error	T <sub>A</sub> = –40°C to +125°C	–0.07		+0.07	%FSR	
	T <sub>A</sub> = –40°C to +85°C	–0.06		+0.06	%FSR	
	T <sub>A</sub> = +25°C	–0.04	±0.01	+0.04	%FSR	
Gain error temperature coefficient			±3		ppm FSR/°C	
Full-scale error	T <sub>A</sub> = –40°C to +125°C	–0.07		+0.07	%FSR	
	T <sub>A</sub> = –40°C to +85°C	–0.06		+0.06	%FSR	
	T <sub>A</sub> = +25°C	–0.04	±0.01	+0.04	%FSR	
Full-scale error temperature coefficient			±1		ppm FSR/°C	

(1) When powered with AVSS = 0 V, INL and offset error for the 0-V to 5-V and 0-V to 10-V ranges are calculated beginning from code 0x0100 for DAC8760 and from code 0x0010 for DAC7760.

(2) Assumes a footroom of 0.5 V.

## ELECTRICAL CHARACTERISTICS (continued)

At AVDD = +10 V to +36 V, AVSS = –18 V to 0 V, AVDD + |AVSS| ≤ 36 V, GND = 0 V, REFIN = +5-V external, and DVDD = +2.7 V to +5.5 V. For VOUT: R<sub>L</sub> = 1 kΩ, C<sub>L</sub> = 200 pF; for IOUT: R<sub>L</sub> = 300 Ω. All specifications are from –40°C to +125°C, unless otherwise noted. Typical specifications are at +25°C.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
<b>VOLTAGE OUTPUT (for Unipolar and Bipolar Modes)</b>						
Headroom	AVDD with respect to VOUT full scale	0.5			V	
Footroom	AVSS with respect to VOUT zero scale	–0.5			V	
Output voltage drift vs time	T <sub>A</sub> = +125°C, 1000 hrs		±15		ppm FSR	
Short-circuit current			30		mA	
Load	For specified performance	1			kΩ	
Capacitive load stability <sup>(3)</sup>	R <sub>L</sub> = ∞			20	nF	
	R <sub>L</sub> = 1 kΩ			5	nF	
	R <sub>L</sub> = 1 kΩ, external compensation capacitor (4 nF) connected			1	μF	
DC output impedance	Code = 0x8000		0.3		Ω	
DC PSRR <sup>(3)</sup>	No output load		3	10	μV/V	
<b>CURRENT OUTPUT</b>						
Output current ranges		0		24	mA	
		0		20	mA	
		4		20	mA	
Resolution	DAC8760	16			Bits	
	DAC7760	12			Bits	
<b>Accuracy (for 0-mA to 20-mA and 0-mA to 24-mA range settings)<sup>(4)</sup></b>						
Total unadjusted error, TUE	T <sub>A</sub> = –40°C to +125°C	–0.2		+0.2	%FSR	
	T <sub>A</sub> = –40°C to +85°C	–0.16		+0.16	%FSR	
	T <sub>A</sub> = +25°C	–0.08	±0.02	+0.08	%FSR	
Differential nonlinearity, DNL	Monotonic			±1	LSB	
Relative accuracy, INL <sup>(5)</sup>	T <sub>A</sub> = –40°C to +125°C			±0.080	%FSR	
	T <sub>A</sub> = –40°C to +85°C			±0.024	%FSR	
Offset error	T <sub>A</sub> = –40°C to +125°C	–0.17		+0.17	%FSR	
	T <sub>A</sub> = –40°C to +85°C	–0.1		+0.1	%FSR	
	T <sub>A</sub> = +25°C	–0.07	±0.01	+0.07	%FSR	
Offset error temperature coefficient			±5		ppm FSR/°C	
Full-scale error	T <sub>A</sub> = –40°C to +125°C	–0.2		+0.2	%FSR	
	T <sub>A</sub> = –40°C to +85°C	–0.16		+0.16	%FSR	
	T <sub>A</sub> = +25°C	–0.08	±0.015	+0.08	%FSR	
Full-scale error temperature coefficient	Internal R <sub>SET</sub>			±5	ppm FSR/°C	
	External R <sub>SET</sub>			±10	ppm FSR/°C	
Gain error	Internal R <sub>SET</sub>	–40°C to +125°C		–0.2	+0.2	%FSR
		–40°C to +85°C		–0.15	+0.15	%FSR
		T <sub>A</sub> = +25°C		–0.08	±0.01	+0.08
	External R <sub>SET</sub>	–40°C to +125°C		–0.17	+0.17	%FSR
		–40°C to +85°C		–0.12	+0.12	%FSR
		T <sub>A</sub> = +25°C		–0.05	±0.01	+0.05
Gain error temperature coefficient	Internal R <sub>SET</sub>			±3	ppm FSR/°C	
	External R <sub>SET</sub>			±8	ppm FSR/°C	
Output current drift vs time	Internal R <sub>SET</sub>	T <sub>A</sub> = +125°C, 1000 hrs		±50		ppm FSR
	External R <sub>SET</sub>			±25		ppm FSR

(3) Specified by design and characterization; not production tested.

(4) DAC8760 and DAC7760 current output range is set by writing to RANGE bits in control register at address 0x55.

(5) For 0-mA to 20-mA and 0-mA to 24-mA ranges, INL is calculated beginning from code 0x0100 for DAC8760 and from code 0x0010 for DAC7760.

## ELECTRICAL CHARACTERISTICS (continued)

At AVDD = +10 V to +36 V, AVSS = –18 V to 0 V, AVDD + |AVSS| ≤ 36 V, GND = 0 V, REFIN = +5-V external, and DVDD = +2.7 V to +5.5 V. For VOUT: R<sub>L</sub> = 1 kΩ, C<sub>L</sub> = 200 pF; for IOUT: R<sub>L</sub> = 300 Ω. All specifications are from –40°C to +125°C, unless otherwise noted. Typical specifications are at +25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Accuracy (for 4-mA to 20-mA range setting)<sup>(6)</sup></b>						
Total unadjusted error, TUE	Internal R <sub>SET</sub>	T <sub>A</sub> = –40°C to +125°C	–0.25		+0.25	%FSR
		T <sub>A</sub> = +25°C	–0.08	±0.02	+0.08	%FSR
	External R <sub>SET</sub>	T <sub>A</sub> = –40°C to +125°C	–0.29		+0.29	%FSR
		T <sub>A</sub> = –40°C to +85°C	–0.25		+0.25	%FSR
		T <sub>A</sub> = +25°C	–0.1	±0.02	+0.1	%FSR
Differential nonlinearity, DNL		Monotonic			±1	LSB
Relative accuracy, INL <sup>(7)</sup>		T <sub>A</sub> = –40°C to +125°C			±0.080	%FSR
		T <sub>A</sub> = –40°C to +85°C			±0.024	%FSR
Offset error	Internal R <sub>SET</sub>	T <sub>A</sub> = –40°C to +125°C	–0.22		+0.22	%FSR
		T <sub>A</sub> = –40°C to +85°C	–0.2		+0.2	%FSR
	External R <sub>SET</sub>	T <sub>A</sub> = –40°C to +125°C	–0.2		+0.2	%FSR
		T <sub>A</sub> = –40°C to +85°C	–0.18		+0.18	%FSR
	Internal and External R <sub>SET</sub>	T <sub>A</sub> = +25°C	–0.07	±0.01	+0.07	%FSR
Offset error temperature coefficient				±3		ppm FSR/°C
Full-scale error	Internal R <sub>SET</sub>	T <sub>A</sub> = –40°C to +125°C	–0.25		+0.25	%FSR
		T <sub>A</sub> = +25°C	–0.08	±0.015	+0.08	%FSR
	External R <sub>SET</sub>	T <sub>A</sub> = –40°C to +125°C	–0.29		+0.29	%FSR
		T <sub>A</sub> = –40°C to +85°C	–0.25		+0.25	%FSR
		T <sub>A</sub> = +25°C	–0.1	±0.015	+0.1	%FSR
Full-scale error temperature coefficient	Internal R <sub>SET</sub>			±5		ppm FSR/°C
	External R <sub>SET</sub>			±10		ppm FSR/°C
Gain error	Internal R <sub>SET</sub>	T <sub>A</sub> = –40°C to +125°C	–0.2		+0.2	%FSR
		T <sub>A</sub> = –40°C to +85°C	–0.15		+0.15	%FSR
		T <sub>A</sub> = +25°C	–0.08	±0.01	+0.08	%FSR
	External R <sub>SET</sub>	T <sub>A</sub> = –40°C to +125°C	–0.16		+0.16	%FSR
		T <sub>A</sub> = –40°C to +85°C	–0.12		+0.12	%FSR
		T <sub>A</sub> = +25°C	–0.05	±0.01	+0.05	%FSR
Gain error temperature coefficient	Internal R <sub>SET</sub>			±3		ppm FSR/°C
	External R <sub>SET</sub>			±8		ppm FSR/°C
Output current drift vs time	Internal R <sub>SET</sub>	T <sub>A</sub> = +125°C, 1000 hrs		±50		ppm FSR
	External R <sub>SET</sub>			±75		ppm FSR
<b>CURRENT OUTPUT CHARACTERISTICS<sup>(8)</sup></b>						
Loop compliance voltage <sup>(9)</sup>	Output = 24 mA				AVDD – 2	V
Inductive load				50		mH
DC PSRR					1	μA/V
Output impedance	Code = 0x8000			50		MΩ
<b>EXTERNAL REFERENCE INPUT</b>						
Reference input voltage			4.95	5	5.05	V
External reference current	REFIN = 5.0 V, outputs off or IOUT enabled			30		μA
Reference input capacitance				10		pF

(6) DAC8760 and DAC7760 current output range is set by writing to RANGE bits in control register at address 0x55.

(7) For 0-mA to 20-mA and 0-mA to 24-mA ranges, INL is calculated beginning from code 0x0100 for DAC8760 and from code 0x0010 for DAC7760.

(8) Specified by design and characterization; not production tested.

(9) Loop compliance voltage is defined as the voltage at the IOUT pin.

## ELECTRICAL CHARACTERISTICS (continued)

At AVDD = +10 V to +36 V, AVSS = –18 V to 0 V, AVDD + |AVSS| ≤ 36 V, GND = 0 V, REFIN = +5-V external, and DVDD = +2.7 V to +5.5 V. For VOUT: R<sub>L</sub> = 1 kΩ, C<sub>L</sub> = 200 pF; for IOUT: R<sub>L</sub> = 300 Ω. All specifications are from –40°C to +125°C, unless otherwise noted. Typical specifications are at +25°C.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>INTERNAL REFERENCE OUTPUT</b>					
Reference output	T <sub>A</sub> = +25°C	4.995		5.005	V
Reference temperature coefficient <sup>(10)</sup>	T <sub>A</sub> = –40°C to +85°C			±10	ppm/°C
Output noise (0.1 Hz to 10 Hz)	T <sub>A</sub> = +25°C		14		μV <sub>PP</sub>
Noise spectral density	T <sub>A</sub> = +25°C, 10 kHz		185		nV/√Hz
Capacitive load			600		nF
Load current			±5		mA
Short-circuit current (REFOUT shorted to GND)			25		mA
Load regulation	AVDD = 24 V, AVSS = 0 V, T <sub>A</sub> = +25°C, sourcing		55		μV/mA
	AVDD = 24 V, AVSS = 0 V, T <sub>A</sub> = +25°C, sinking		120		μV/mA
Line regulation			±1.2		μV/V
<b>DVDD INTERNAL REGULATOR</b>					
Output voltage	AVDD = 24 V		4.6		V
Output load current <sup>(10)</sup>				10	mA
Load regulation			3.5		mV/mA
Line regulation			1		mV/V
Short-circuit current	AVDD = 24 V, to GND		35		mA
Capacitive load stability <sup>(10)</sup>				2.5	μF
<b>DIGITAL INPUTS</b>					
V <sub>IH</sub> , input high voltage		2			V
V <sub>IL</sub> , input low voltage	3.6 V < AVDD < 5.5 V			0.8	V
	2.7 V < AVDD < 3.6 V			0.6	V
Hysteresis voltage			0.4		V
Input current	DVDD-EN, V <sub>IN</sub> ≤ 5 V	–2.7			μA
	All pins other than DVDD-EN			±1	μA
Pin capacitance	Per pin		10		pF
<b>DIGITAL OUTPUTS</b>					
SDO	V <sub>OL</sub> , output low voltage	Sinking 200 μA		0.4	V
	V <sub>OH</sub> , output high voltage	Sourcing 200 μA	DVDD – 0.5		V
	High-impedance leakage			±1	μA
ALARM	V <sub>OL</sub> , output low voltage	10-kΩ pull-up resistor to DVDD		0.4	V
	V <sub>OL</sub> , output low voltage	2.5 mA		0.6	V
	High-impedance leakage			±1	μA
High-impedance output capacitance			10		pF

(10) Specified by design and characterization; not production tested.

## ELECTRICAL CHARACTERISTICS (continued)

At AVDD = +10 V to +36 V, AVSS = –18 V to 0 V, AVDD + |AVSS| ≤ 36 V, GND = 0 V, REFIN = +5-V external, and DVDD = +2.7 V to +5.5 V. For VOUT: R<sub>L</sub> = 1 kΩ, C<sub>L</sub> = 200 pF; for IOUT: R<sub>L</sub> = 300 Ω. All specifications are from –40°C to +125°C, unless otherwise noted. Typical specifications are at +25°C.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>POWER REQUIREMENTS</b>					
AVDD	AVDD +  AVSS  ≤ 36 V	10		36	V
AVSS	AVDD +  AVSS  ≤ 36 V	–18		0	V
DVDD	Internal regulator disabled	2.7		5.5	V
AIDD	Outputs disabled, external DVDD			3	mA
	Outputs disabled, internal DVDD			4	
	Code = 0x8000, VOUT enabled, unloaded			4.6	
	Code = 0x0000, IOUT enabled			3	
	Code = 0x0000, both outputs enabled, VOUT unloaded			4.6	
AISS	Outputs disabled			0.6	mA
	Outputs disabled, Internal DVDD			0.6	
	Code = 0x8000, VOUT enabled, unloaded			2.6	
	Code = 0x0000, IOUT enabled			0.6	
	Code = 0x0000, both outputs enabled, VOUT unloaded			2.6	
DIDD	V <sub>IH</sub> = DVDD, V <sub>IL</sub> = GND, interface idle			1	mA
Power dissipation	AVDD = 36 V, AVSS = GND, VOUT enabled, unloaded, DVDD = 5 V		140	170	mW
	AVDD = 18 V, AVSS = –18 V, VOUT enabled, unloaded, DVDD = 5 V			135	
<b>TEMPERATURE</b>					
Specified performance range		–40		+125	°C
Thermal alarm			142		°C
Thermal alarm hysteresis			18		°C

### ELECTRICAL CHARACTERISTICS: AC

At AVDD = +10 V to +36 V, AVSS = –18 V to 0 V, AVDD + |AVSS| ≤ 36 V, GND = 0 V, REFIN = +5-V external; and DVDD = +4.5 V to +5.5 V. For VOUT: R<sub>L</sub> = 2 kΩ, C<sub>L</sub> = 200 pF; for IOUT: R<sub>L</sub> = 300 Ω. All specifications –40°C to +125°C, unless otherwise noted. Typical specifications are at +25°C.

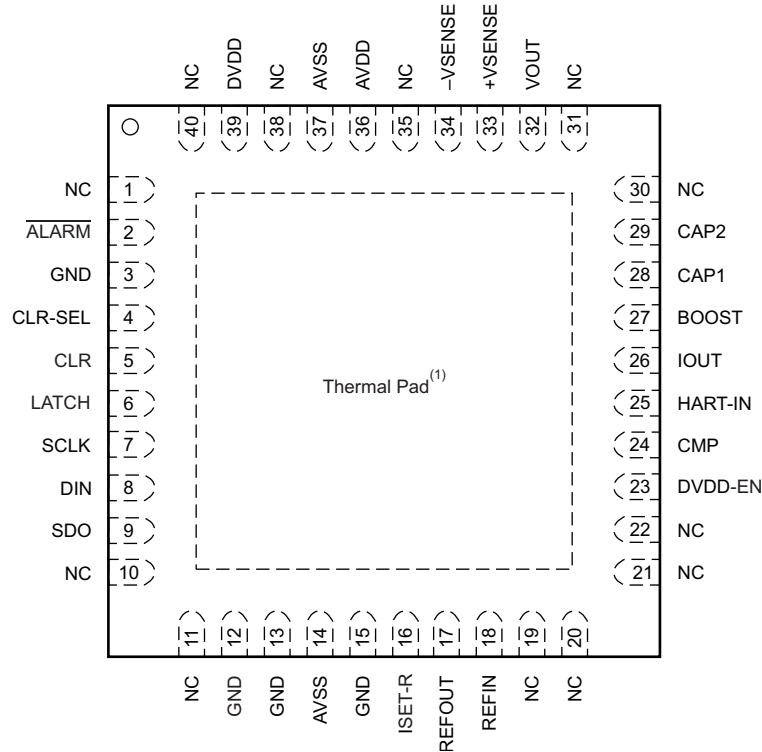
PARAMETER <sup>(1)</sup>	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>DYNAMIC PERFORMANCE</b>					
<b>CURRENT OUTPUT</b>					
Output current settling time	16-mA step, to 0.1% FSR, no L (inductance)		10		μs
	16-mA step, to 0.1% FSR, L < 1 mH		25		μs
AC PSRR	200-mV, 50-Hz or 60-Hz sine wave superimposed on power-supply voltage		–75		dB
<b>VOLTAGE OUTPUT</b>					
Output voltage settling time	0 V to 10 V, to ±0.03% FSR		22		μs
	0 V to 5 V, to ±0.03% FSR		13		μs
Slew rate			0.5		V/μs
Power-on glitch energy			2.5		μV-s
Digital-to-analog glitch energy			0.4		μV-s
Glitch impulse peak amplitude			200		mV
Digital feedthrough			2		nV-s
Output noise (0.1-Hz to 10-Hz bandwidth)			0.1		LSB <sub>pp</sub>
1 / f corner frequency			100		Hz
Output noise spectral density	Measured at 10 kHz		180		nV/√Hz
AC PSRR	200-mV, 50-Hz or 60-Hz sine wave superimposed on power-supply voltage		–75		dB

(1) Specified by characterization, not production tested.

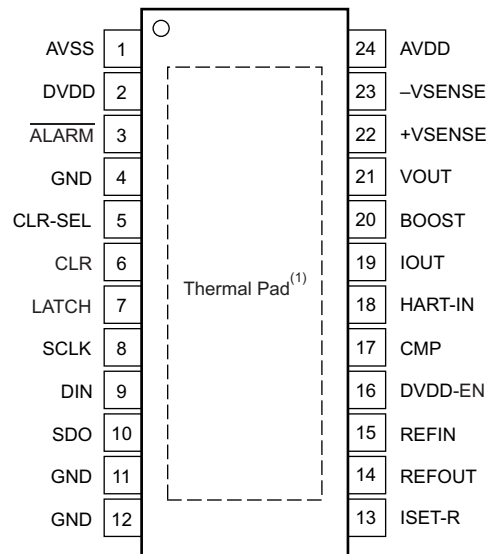


## PIN CONFIGURATIONS

### RHA PACKAGE QFN-40 (TOP VIEW)



### PWP PACKAGE TSSOP-24 (TOP VIEW)



(1) Thermal pad connected to AVSS.

**PIN DESCRIPTIONS**

NAME	QFN NO.	TSSOP NO.	DESCRIPTION
ALARM	2	3	Alarm pin. Open drain output. External pullup resistor required (10 kΩ). The pin goes low (active) when the ALARM condition is detected (open circuit, over temperature, timeout and so forth).
AVDD	36	24	Positive analog power supply.
AVSS	14, 37	1	Negative analog power supply in dual power-supply operation. Connects to GND in single power-supply operation.
BOOST	27	20	Boost pin. External transistor connection (optional).
CAP1	28	—	Connection for current output filtering capacitor (optional).
CAP2	29	—	Connection for current output filtering capacitor (optional).
CLR	5	6	Clear input. Logic high on this pin causes the part to enter CLEAR state. Active high.
CLR-SEL	4	5	Selects the VOUT value in CLEAR state, after power-on and reset.
CMP	24	17	External compensation capacitor connection pin (optional). Addition of the external capacitor (connected between VOUT and this pin) improves the stability with high capacitive loads at the VOUT pin by reducing the bandwidth of the output amplifier, thus increasing the settling time.
DIN	8	9	Serial data input. Data are clocked into the 24-bit input shift register on the rising edge of the serial clock input. Schmitt-Trigger logic input.
DVDD	39	2	Digital power supply. Can be input or output, depending on DVDD-EN pin.
DVDD-EN	23	16	Internal power-supply enable pin. Connect this pin to GND to disable the internal supply, or leave this pin unconnected to enable the internal supply. When this pin is connected to GND, an external supply must be connected to the DVDD pin.
GND	3	4	Ground reference point for all digital circuitry of the device. Connects to 0 V.
GND	12, 13, 15	11, 12	Ground reference point for all analog circuitry of the device.
HART-IN	25	18	Input pin for HART modulation.
IOUT	26	19	Current output pin
ISET-R	16	13	Connection pin for external precision resistor (15 kΩ). See the <a href="#">THEORY OF OPERATION</a> section of this data sheet.
LATCH	6	7	Load DAC registers input. A rising edge on this pin loads the input shift register data into the DAC data and control registers and updates the DAC outputs.
NC	1, 10, 11, 19, 20, 21, 22, 30, 31, 35, 38, 40	—	No connection.
REFOUT	17	14	Internal reference output. Connects to REFIN when using internal reference.
REFIN	18	15	Reference input
SCLK	7	8	Serial clock input of serial peripheral interface (SPI™). Data can be transferred at rates up to 30 MHz. Schmitt-Trigger logic input.
SDO	9	10	Serial data output. Data are valid on the rising edge of SCLK.
THERMAL PAD	—	—	The thermal pad is internally connected to the AVSS supply. It is recommended that the pad be thermally connected to a copper plane for enhanced thermal performance. The pad can be electrically connected to the same potential as the AVSS pin (either negative supply voltage or GND) or left electrically unconnected provided a supply connection is made at the AVSS pin. The AVSS pin must always be connected to either the negative supply voltage or GND, independent of the thermal pad connection.
VOUT	32	21	Voltage output pin. This is a buffered analog voltage output.
+VSENSE	33	22	Sense pin for the positive voltage output load connection.
-VSENSE	34	23	Sense pin for the negative voltage output load connection.

## TIMING CHARACTERISTICS

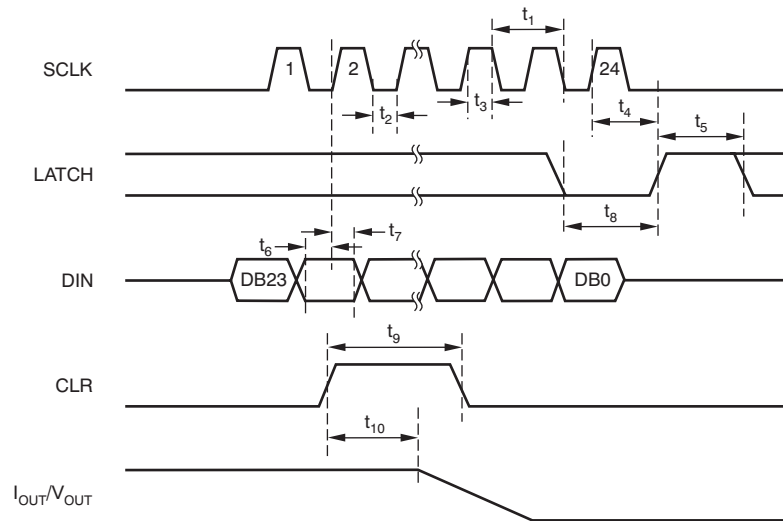


Figure 1. Write Mode Timing

### TIMING REQUIREMENTS: Write Mode

At  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$  and  $DV_{DD} = +2.7\text{ V}$  to  $+5.5\text{ V}$ , unless otherwise noted.

PARAMETER <sup>(1)</sup>		MIN	MAX	UNIT
t <sub>1</sub>	SCLK cycle time	33		ns
t <sub>2</sub>	SCLK low time	13		ns
t <sub>3</sub>	SCLK high time	13		ns
t <sub>4</sub>	LATCH delay time	13		ns
t <sub>5</sub>	LATCH high time <sup>(2)</sup>	40		ns
t <sub>6</sub>	Data setup time	5		ns
t <sub>7</sub>	Data hold time	7		ns
t <sub>8</sub>	LATCH low time	40		ns
t <sub>9</sub>	CLR pulse width	20		ns
t <sub>10</sub>	CLR activation time		5	μs

(1) Specified by design, not production tested.

(2) Based on digital interface circuitry only.

When writing to DAC control and config registers, consider the analog output specifications in [ELECTRICAL CHARACTERISTICS: AC](#).

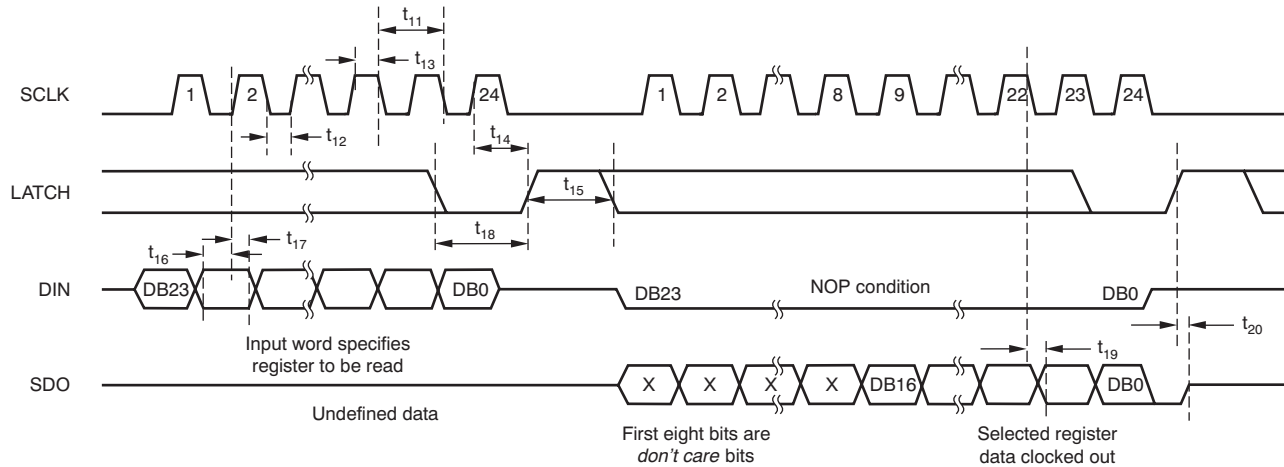


Figure 2. Readback Mode Timing

### TIMING REQUIREMENTS: Readback Mode

At  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$  and  $DV_{DD} = +2.7\text{ V}$  to  $+5.5\text{ V}$ , unless otherwise noted.

PARAMETER <sup>(1)</sup>		MIN	MAX	UNIT
$t_{11}$	SCLK cycle time	60		ns
$t_{12}$	SCLK low time	25		ns
$t_{13}$	SCLK high time	25		ns
$t_{14}$	LATCH delay time	13		ns
$t_{15}$	LATCH high time	40		ns
$t_{16}$	Data setup time	5		ns
$t_{17}$	Data hold time	7		ns
$t_{18}$	LATCH low time	40		ns
$t_{19}$	Serial output delay time ( $C_{L, SDO} = 15\text{ pF}$ )		35	ns
$t_{20}$	LATCH rising edge to SDO 3-state ( $C_{L, SDO} = 15\text{ pF}$ )		35	ns

(1) Specified by design, not production tested.

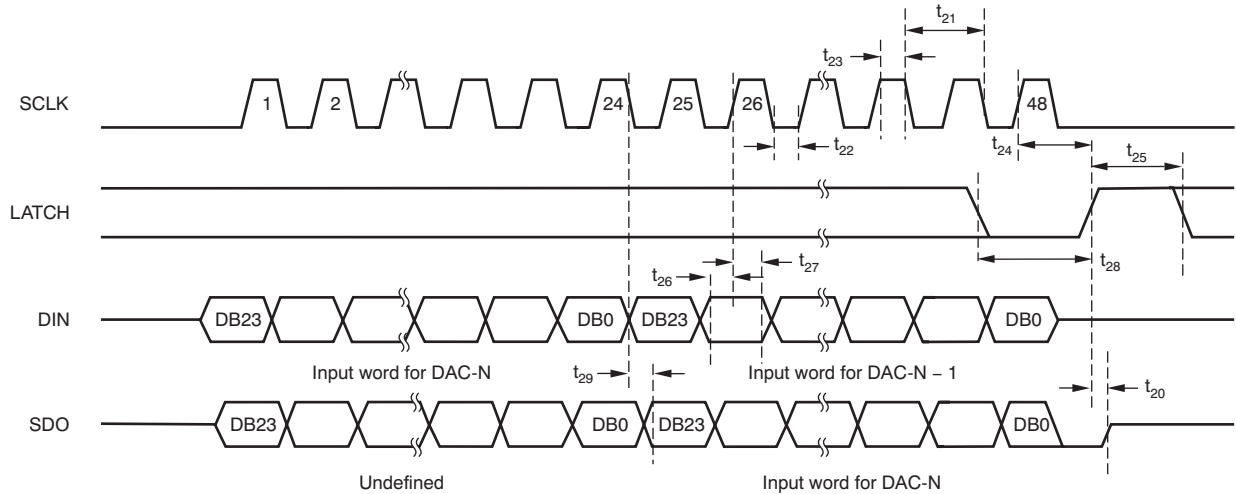


Figure 3. Daisy-Chain Mode Timing

### TIMING REQUIREMENTS: Daisy-Chain Mode

At  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$  and  $DV_{DD} = 2.7 \text{ V}$  to  $5.5 \text{ V}$ , unless otherwise noted.

PARAMETER <sup>(1)</sup>		MIN	MAX	UNIT
$t_{21}$	SCLK cycle time	60		ns
$t_{22}$	SCLK low time	25		ns
$t_{23}$	SCLK high time	25		ns
$t_{24}$	LATCH delay time	13		ns
$t_{25}$	LATCH high time	40		ns
$t_{26}$	Data setup time	5		ns
$t_{27}$	Data hold time	7		ns
$t_{28}$	LATCH low time	40		ns
$t_{29}$	Serial output delay time ( $C_L, SDO = 15 \text{ pF}$ )		35	ns

(1) Specified by design, not production tested.

## TYPICAL CHARACTERISTICS

At  $T_A = +25^\circ\text{C}$ , unless otherwise noted.

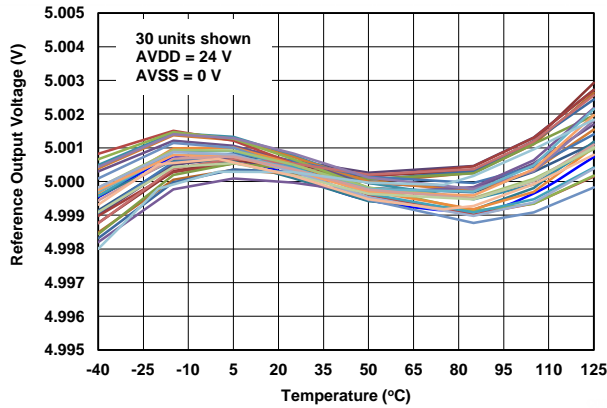


Figure 4. REFOUT vs TEMPERATURE

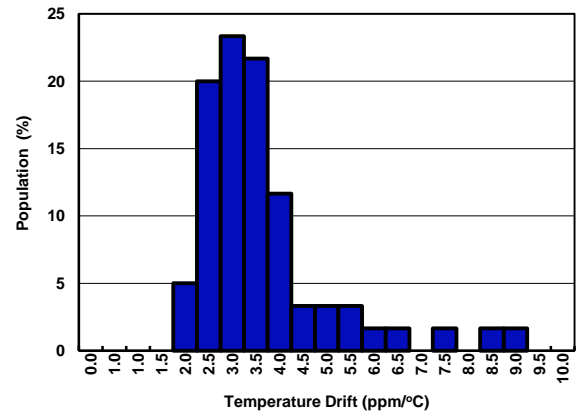


Figure 5. INTERNAL REFERENCE TEMPERATURE DRIFT HISTOGRAM

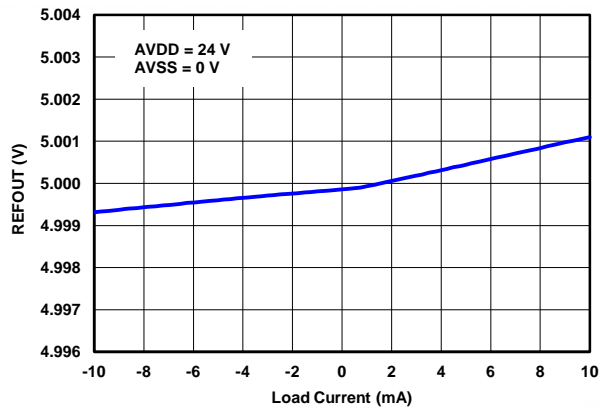


Figure 6. REFOUT vs LOAD CURRENT

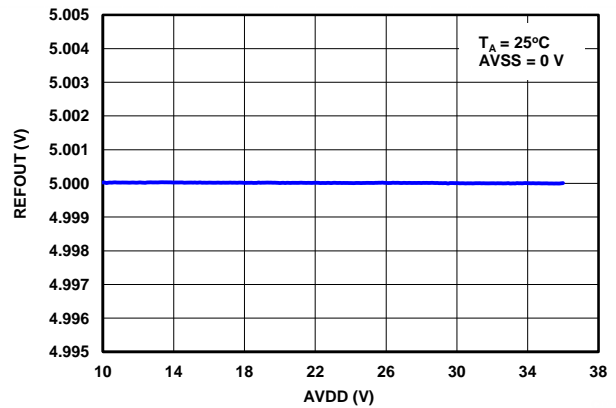


Figure 7. REFOUT vs AVDD

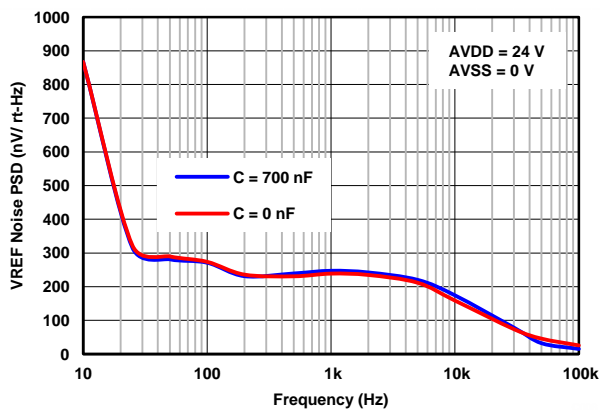


Figure 8. REFOUT NOISE PSD vs FREQUENCY

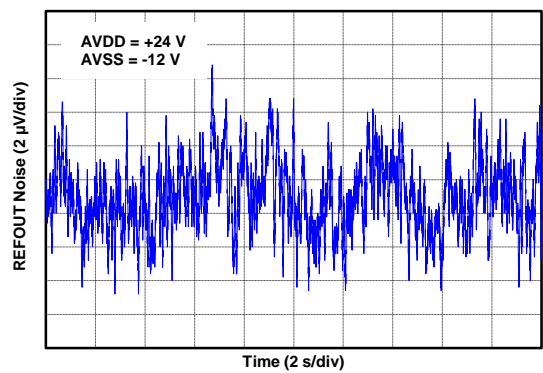


Figure 9. INTERNAL REFERENCE, PEAK-TO-PEAK NOISE (0.1 Hz to 10 Hz)

### TYPICAL CHARACTERISTICS (continued)

At  $T_A = +25^\circ\text{C}$ , unless otherwise noted.

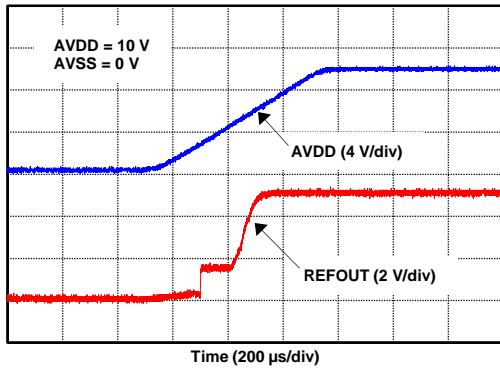


Figure 10. REFOUT TRANSIENT vs TIME

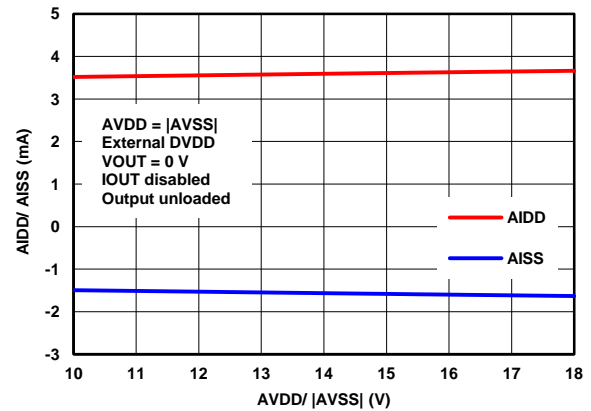


Figure 11. AIDD or AISS vs AVDD or AVSS

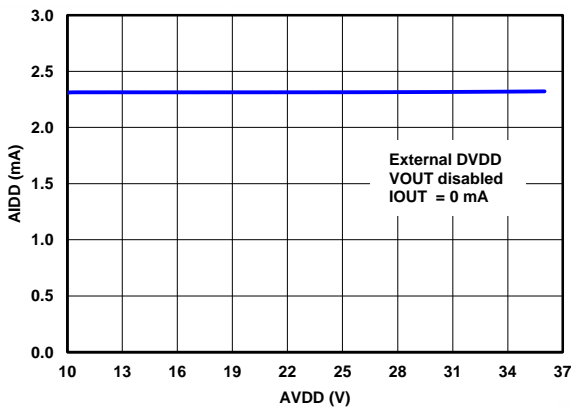


Figure 12. AIDD vs AVDD

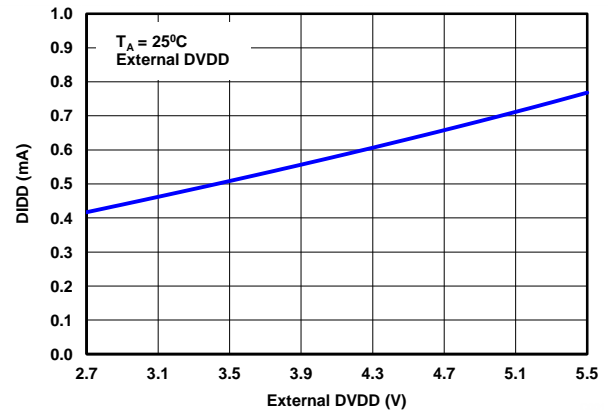


Figure 13. DIDD vs EXTERNAL DVDD

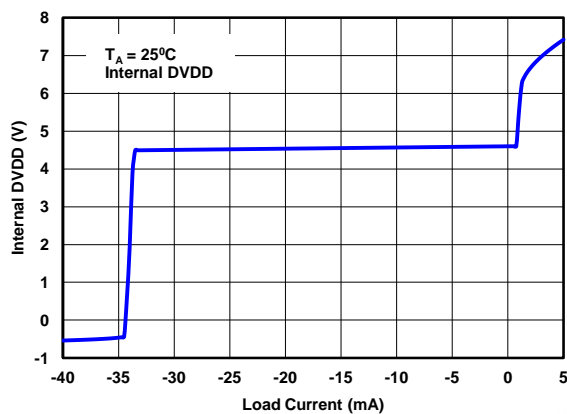


Figure 14. INTERNAL DVDD vs LOAD CURRENT

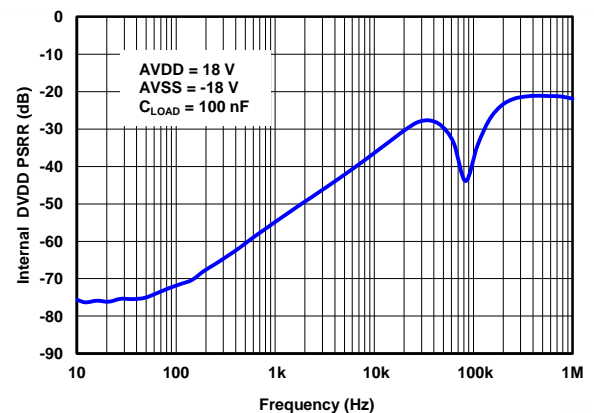


Figure 15. INTERNAL DVDD PSRR vs FREQUENCY

TYPICAL CHARACTERISTICS (continued)

At  $T_A = +25^\circ\text{C}$ , unless otherwise noted.

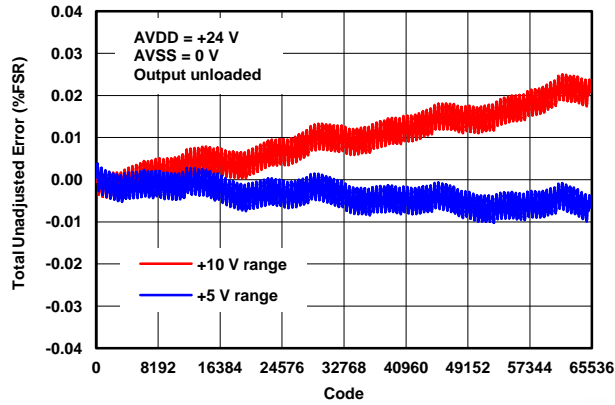


Figure 16. VOUT TUE vs CODE (Unipolar Outputs)

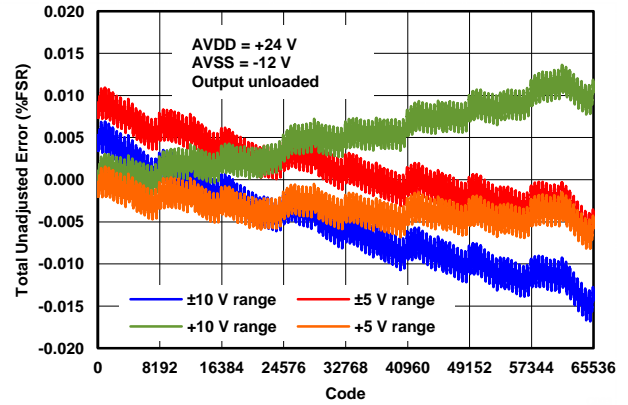


Figure 17. VOUT TUE vs CODE

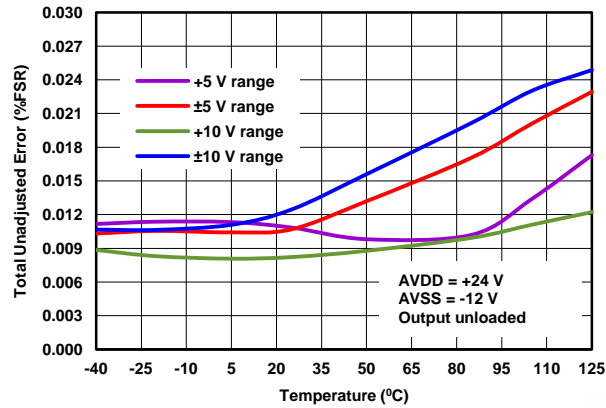


Figure 18. VOUT TUE vs TEMPERATURE

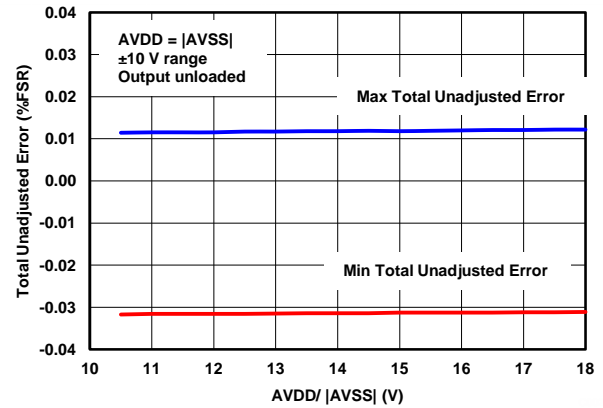


Figure 19. VOUT TUE vs SUPPLY

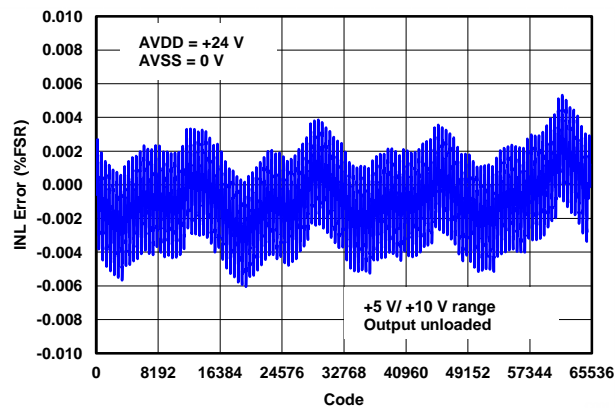


Figure 20. VOUT INL vs CODE (Unipolar Outputs)

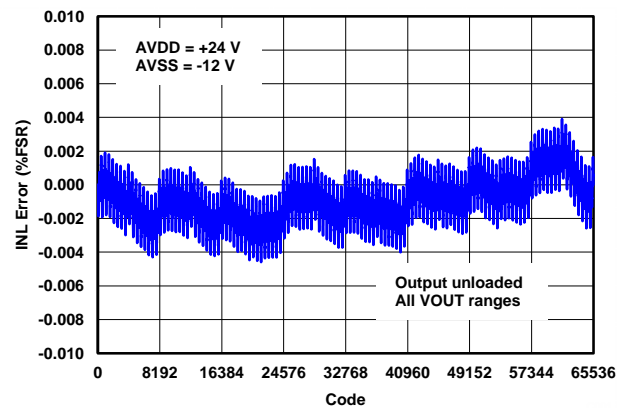


Figure 21. VOUT INL vs CODE



TYPICAL CHARACTERISTICS (continued)

At  $T_A = +25^\circ\text{C}$ , unless otherwise noted.

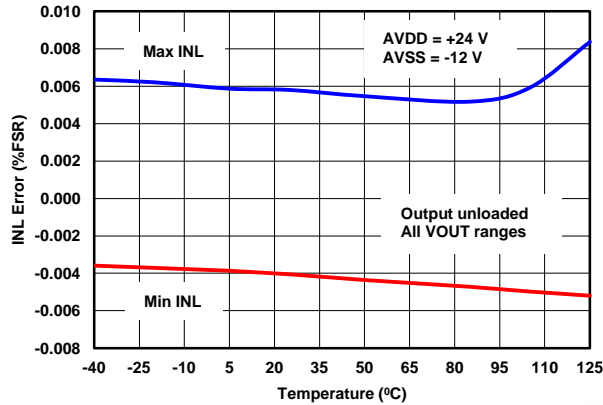


Figure 22. VOUT INL vs TEMPERATURE

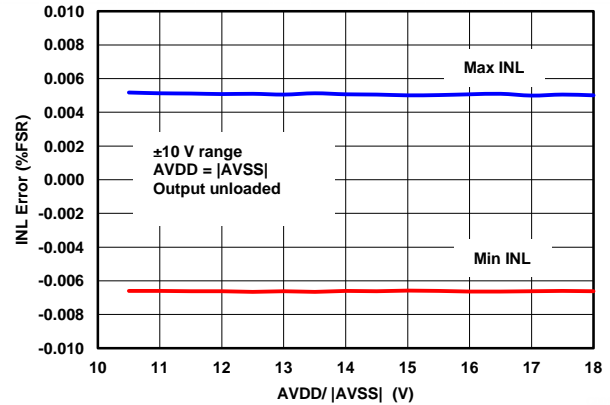


Figure 23. VOUT INL vs SUPPLY

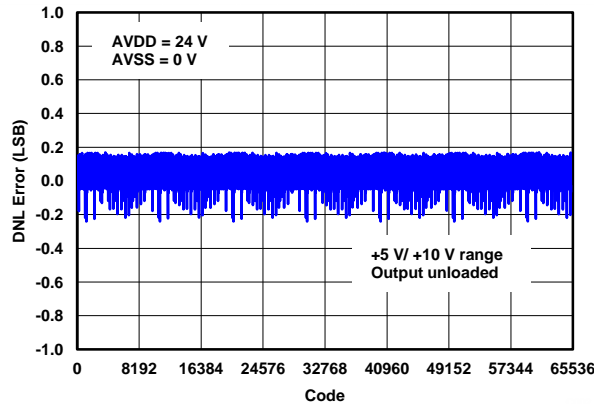


Figure 24. VOUT DNL vs CODE (Unipolar Outputs)

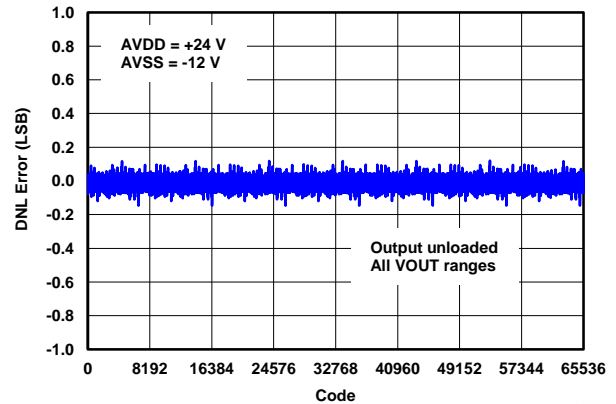


Figure 25. VOUT DNL vs CODE

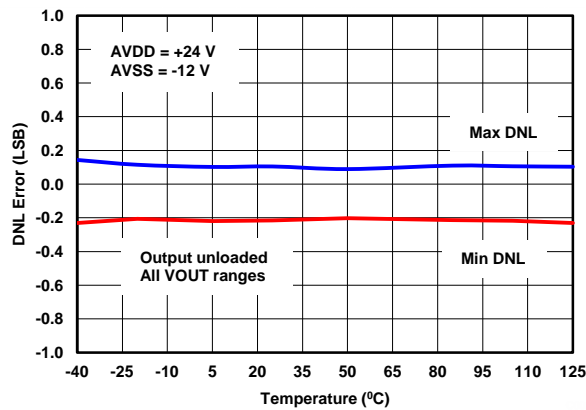


Figure 26. VOUT DNL vs TEMPERATURE

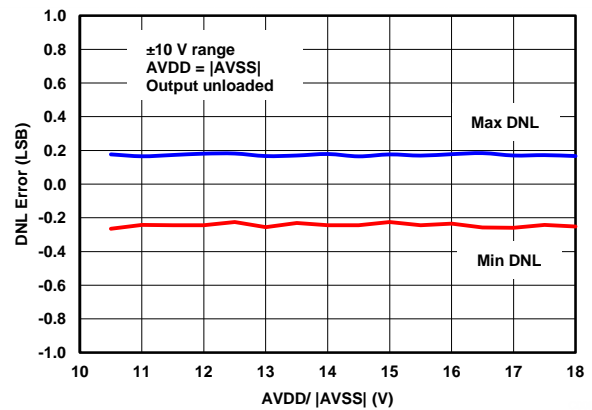


Figure 27. VOUT DNL vs SUPPLY

TYPICAL CHARACTERISTICS (continued)

At  $T_A = +25^\circ\text{C}$ , unless otherwise noted.

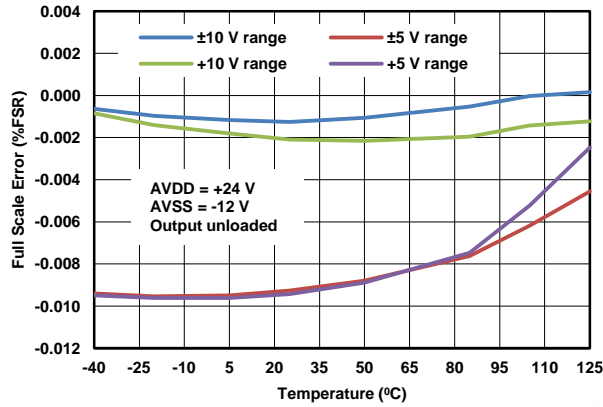


Figure 28. VOUT FULL-SCALE ERROR vs TEMPERATURE

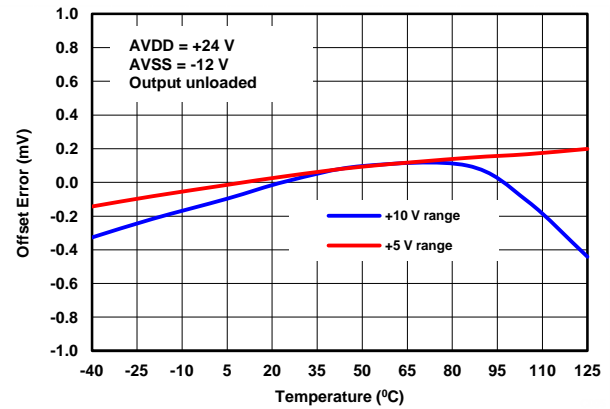


Figure 29. OFFSET ERROR vs TEMPERATURE

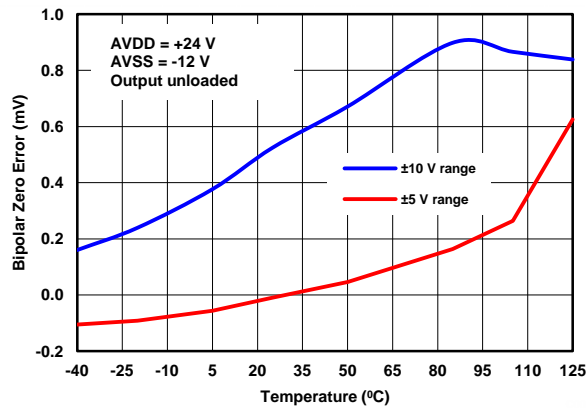


Figure 30. BIPOLAR ZERO ERROR vs TEMPERATURE

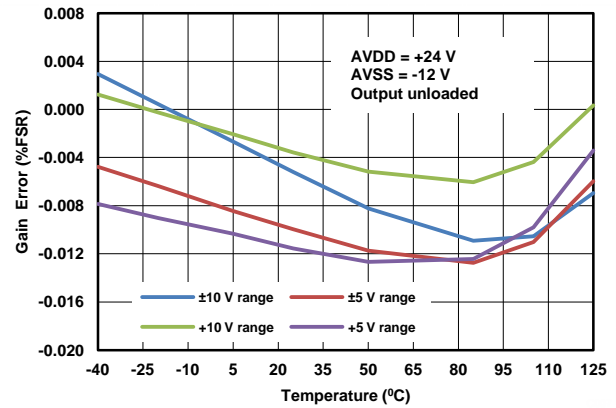


Figure 31. GAIN ERROR vs TEMPERATURE

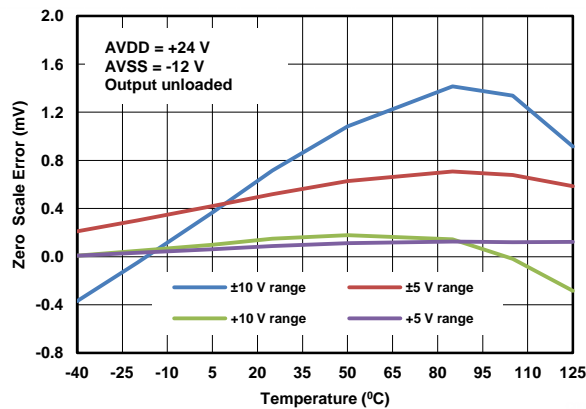


Figure 32. ZERO-SCALE ERROR vs TEMPERATURE

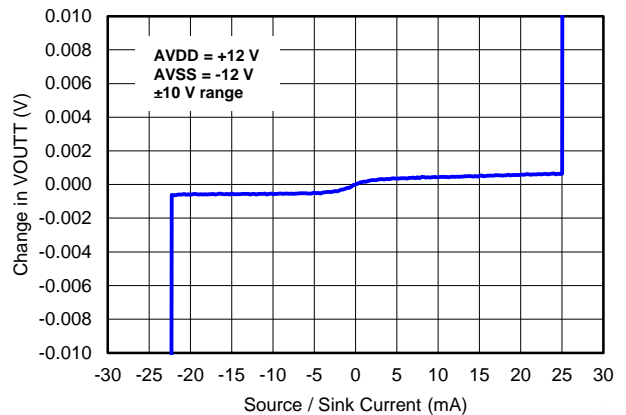


Figure 33. VOUT (Full-Scale) vs LOAD CURRENT (Source or Sink)

TYPICAL CHARACTERISTICS (continued)

At  $T_A = +25^\circ\text{C}$ , unless otherwise noted.

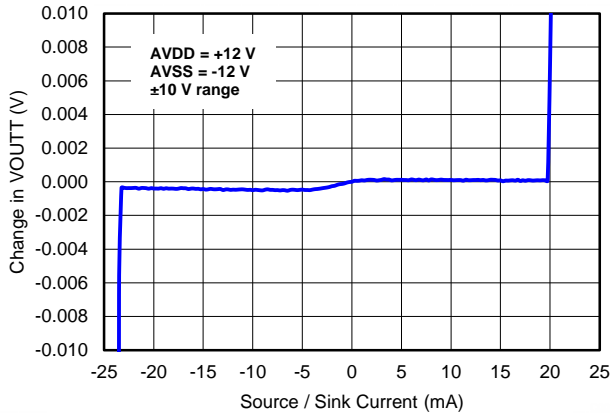


Figure 34. VOUT (Zero-Scale) vs LOAD CURRENT (Source or Sink)

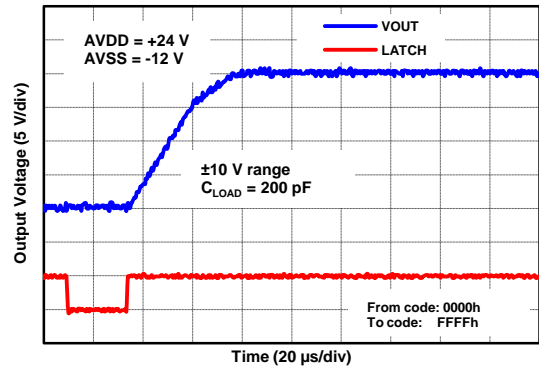


Figure 35. BP10V RISING

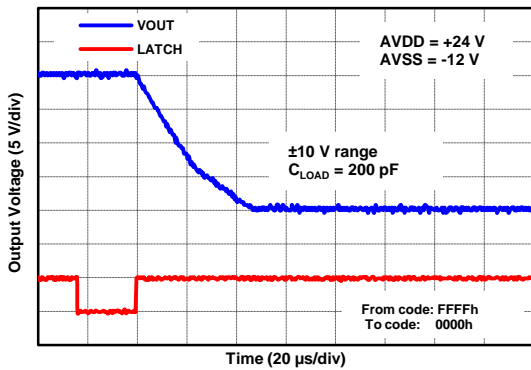


Figure 36. BP10V FALLING

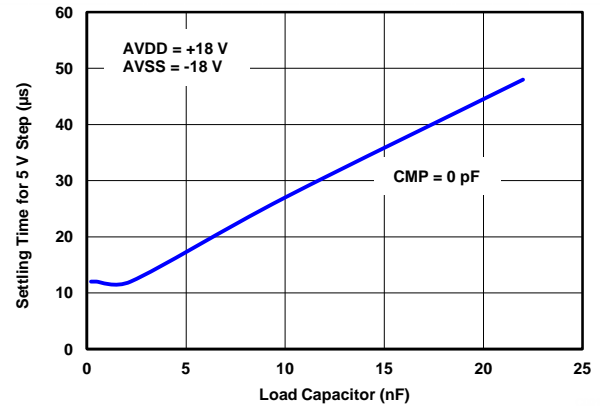


Figure 37. VOUT SETTLING TIME vs LOAD (No Compensation Capacitor)

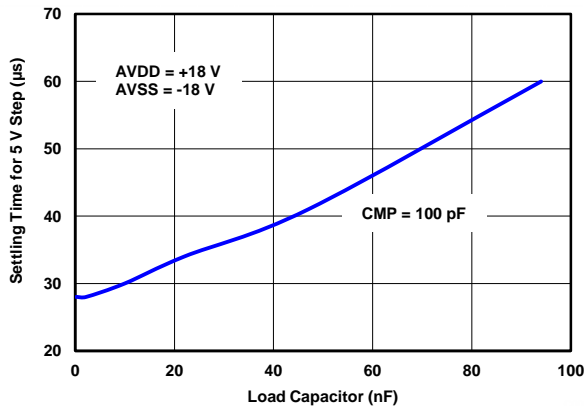


Figure 38. VOUT SETTLING TIME vs LOAD (100 pF Between VOUT and CMP Pins)

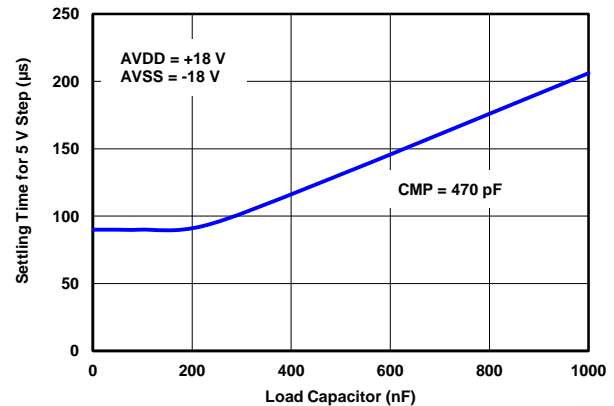


Figure 39. VOUT SETTLING TIME vs LOAD (470 pF Between VOUT and CMP Pins)

**TYPICAL CHARACTERISTICS (continued)**

At  $T_A = +25^\circ\text{C}$ , unless otherwise noted.

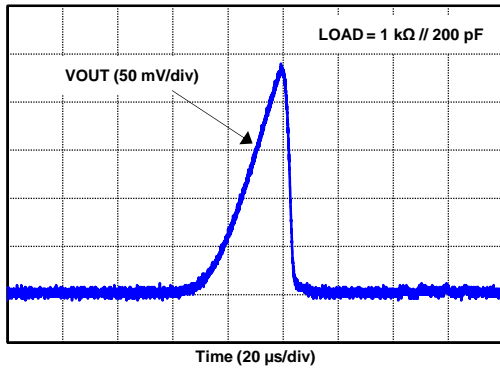


Figure 40. VOUT POWER-ON GLITCH

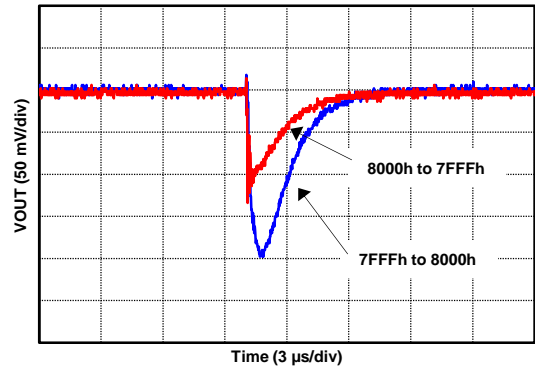


Figure 41. VOUT DIGITAL-TO-ANALOG GLITCH

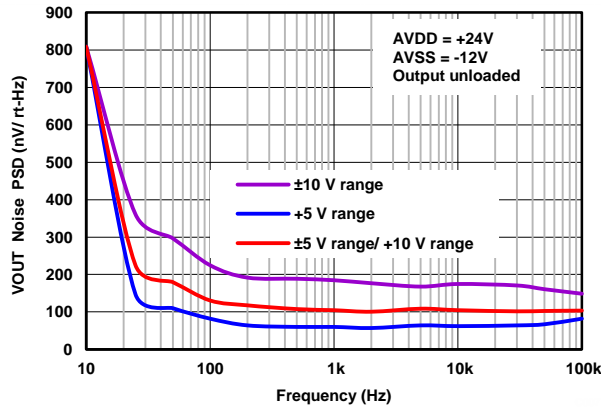


Figure 42. VOUT NOISE PSD vs FREQUENCY

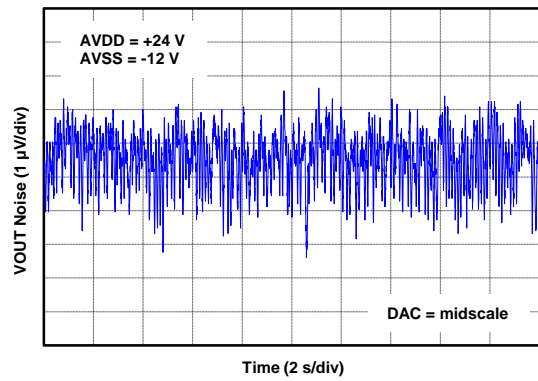


Figure 43. VOUT, PEAK-TO-PEAK NOISE (0.1 Hz to 10 Hz)

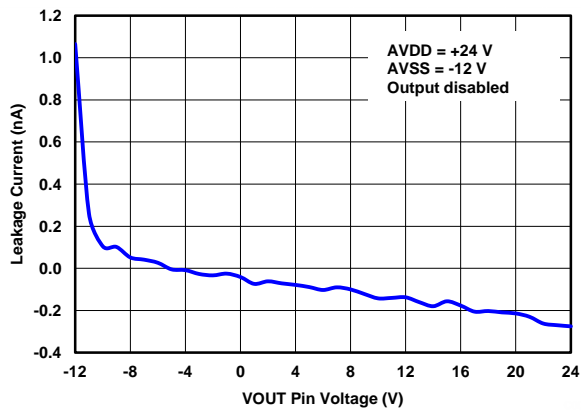


Figure 44. VOUT Hi-Z LEAKAGE CURRENT vs VOLTAGE

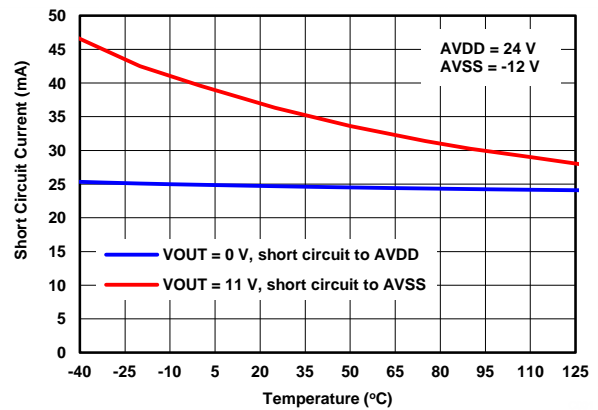


Figure 45. VOUT SHORT-CIRCUIT CURRENT vs TEMPERATURE

TYPICAL CHARACTERISTICS (continued)

At  $T_A = +25^\circ\text{C}$ , unless otherwise noted.

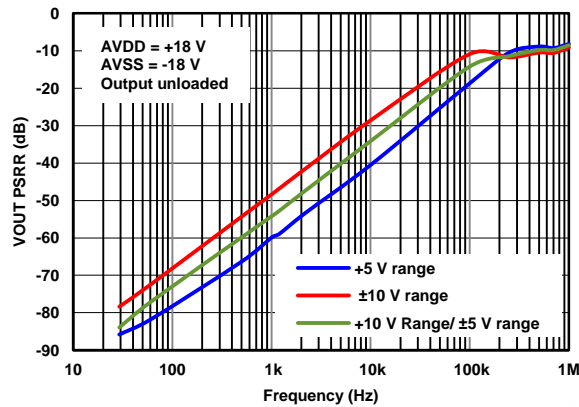


Figure 46. AVDD PSRR FOR VOUT

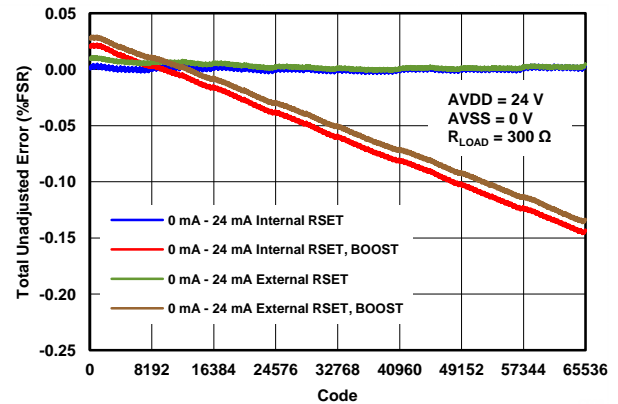


Figure 47. IOU TUE vs CODE (0 mA to 24 mA)

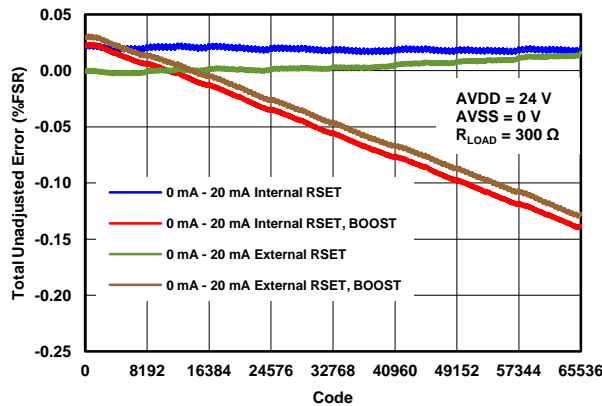


Figure 48. IOU TUE vs CODE (0 mA to 20 mA)

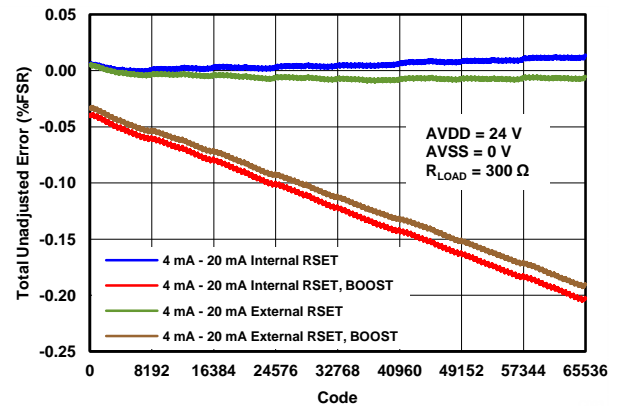


Figure 49. IOU TUE vs CODE (4 mA to 20 mA)

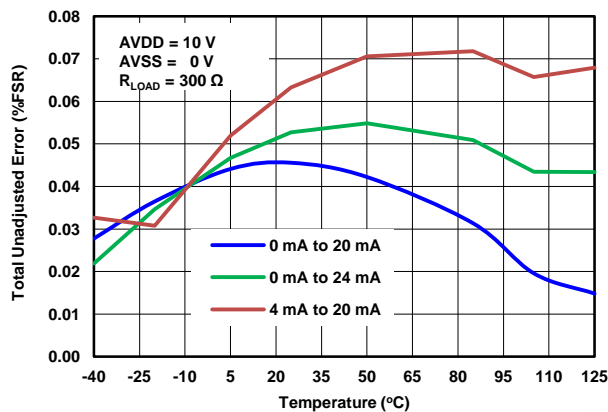


Figure 50. IOU TUE vs TEMPERATURE (Internal  $R_{SET}$ )

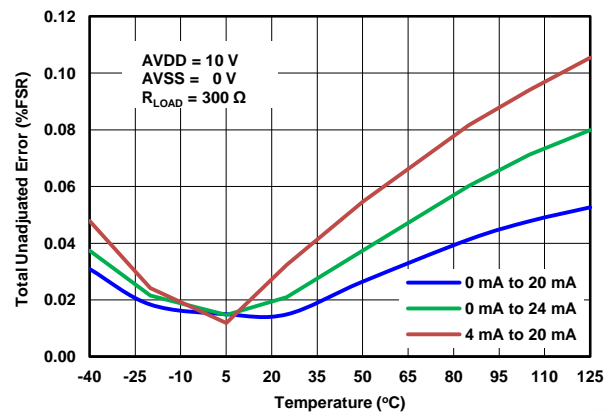


Figure 51. IOU TUE vs TEMPERATURE (External  $R_{SET}$ )

**TYPICAL CHARACTERISTICS (continued)**

At  $T_A = +25^\circ\text{C}$ , unless otherwise noted.

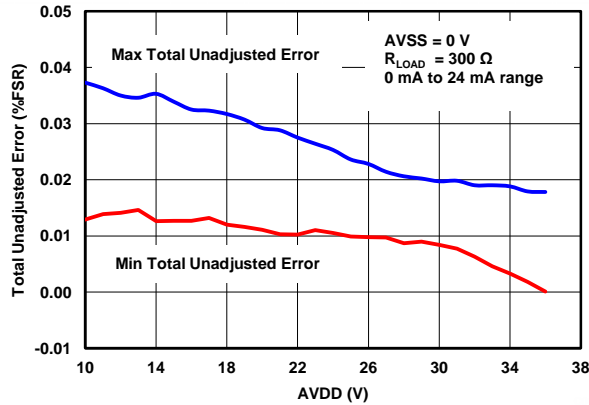


Figure 52. IOUT TUE vs SUPPLY (Internal  $R_{SET}$ )

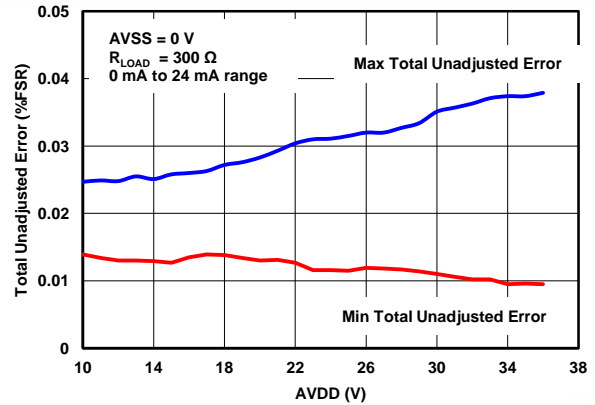


Figure 53. IOUT TUE vs SUPPLY (External  $R_{SET}$ )

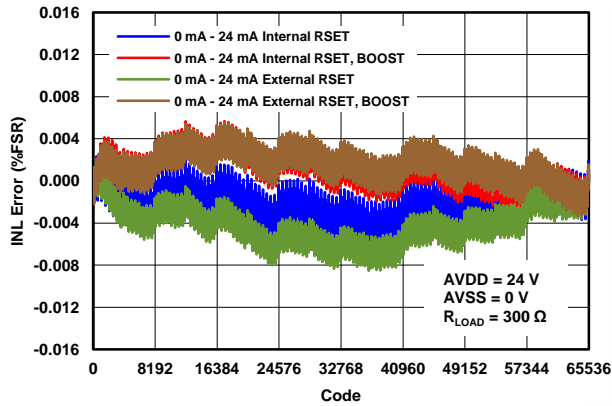


Figure 54. IOUT INL vs CODE (0 mA to 24 mA)

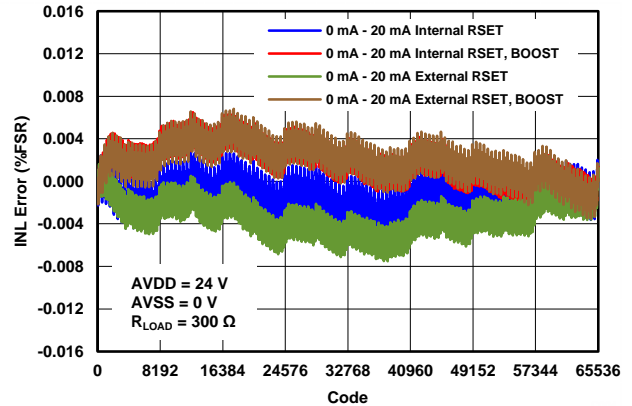


Figure 55. IOUT INL vs CODE (0 mA to 20 mA)

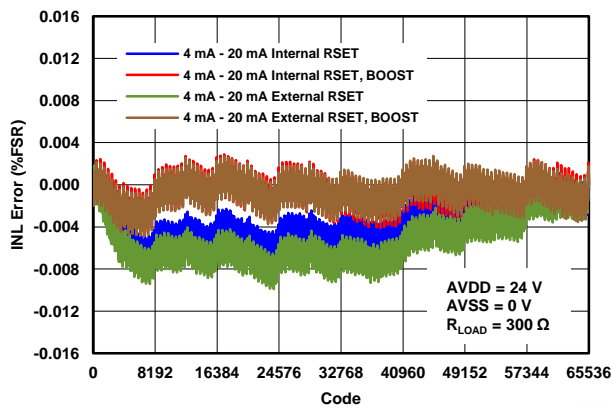


Figure 56. IOUT INL vs CODE (4 mA to 20 mA)

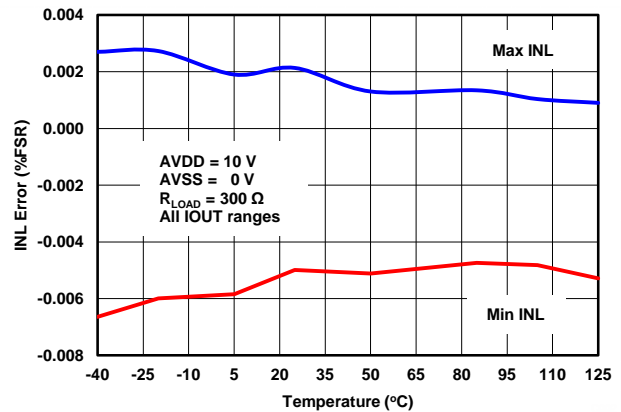


Figure 57. IOUT INL vs TEMPERATURE (Internal  $R_{SET}$ )

TYPICAL CHARACTERISTICS (continued)

At  $T_A = +25^\circ\text{C}$ , unless otherwise noted.

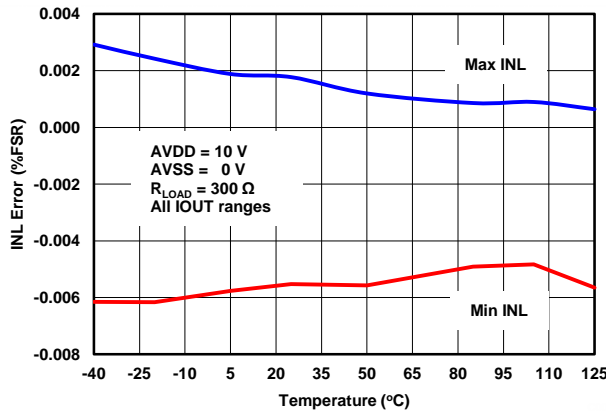


Figure 58. IOUT INL vs TEMPERATURE (External  $R_{SET}$ )

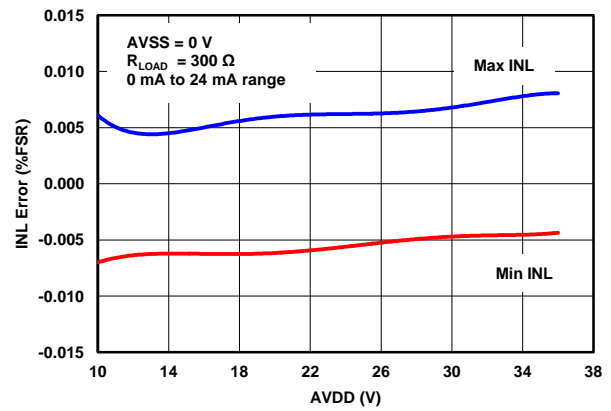


Figure 59. IOUT INL vs SUPPLY (Internal  $R_{SET}$ )

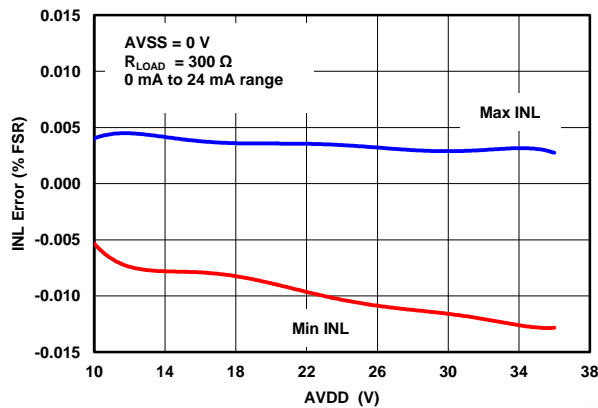


Figure 60. IOUT INL vs SUPPLY (External  $R_{SET}$ )

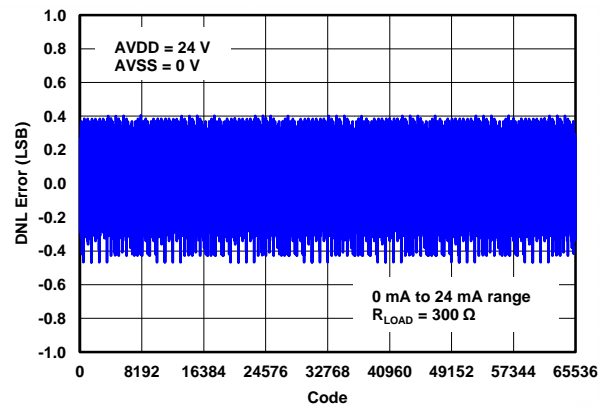


Figure 61. IOUT DNL vs CODE (0 mA to 24 mA)

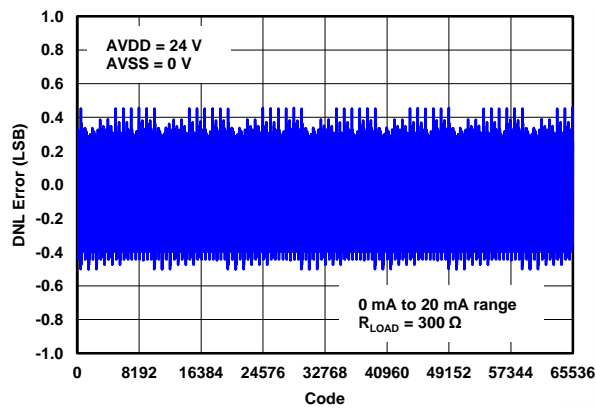


Figure 62. IOUT DNL vs CODE (0 mA to 20 mA)

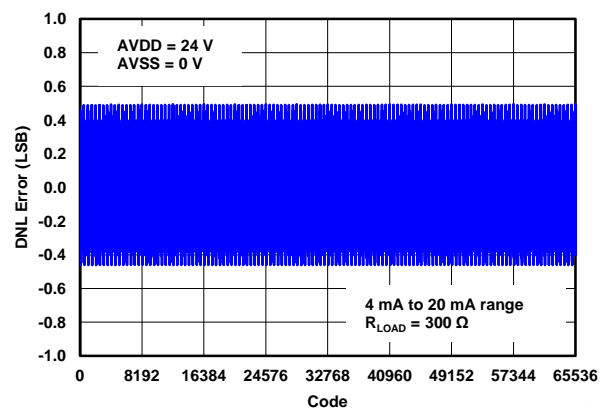


Figure 63. IOUT DNL vs CODE (4 mA to 20 mA)

TYPICAL CHARACTERISTICS (continued)

At  $T_A = +25^\circ\text{C}$ , unless otherwise noted.

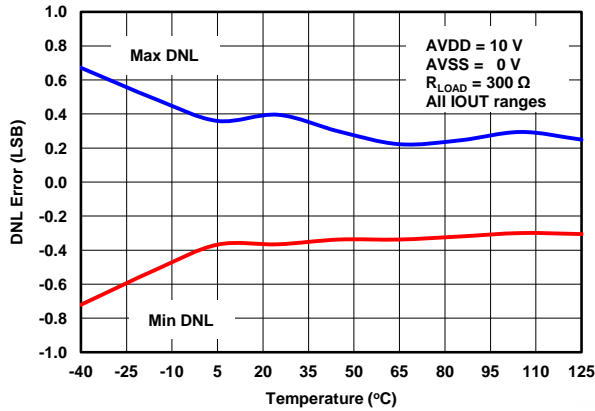


Figure 64. IOUT DNL vs TEMPERATURE (Internal  $R_{SET}$ )

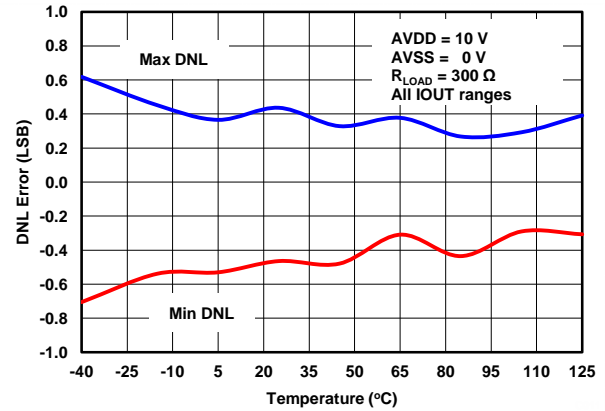


Figure 65. IOUT DNL vs TEMPERATURE (External  $R_{SET}$ )

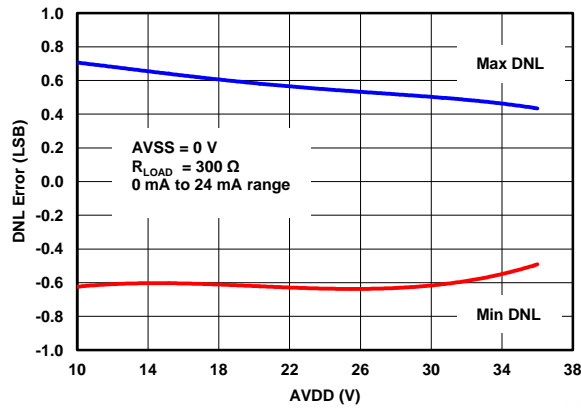


Figure 66. IOUT DNL vs SUPPLY (Internal  $R_{SET}$ )

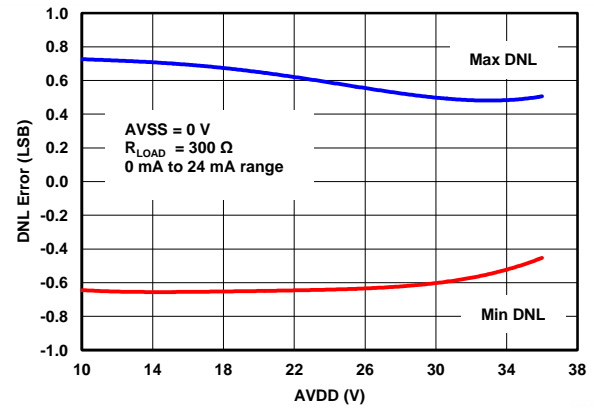


Figure 67. IOUT DNL vs SUPPLY (External  $R_{SET}$ )

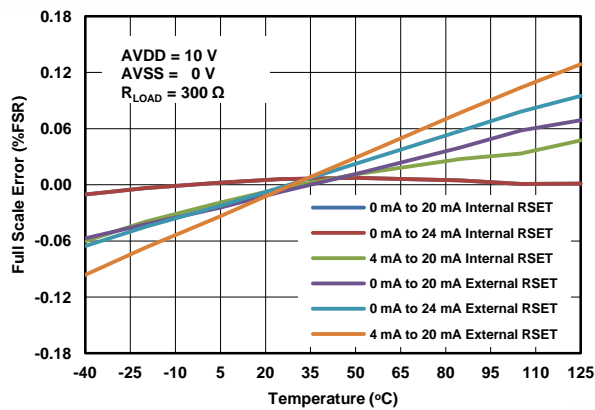


Figure 68. IOUT FULL-SCALE ERROR vs TEMPERATURE

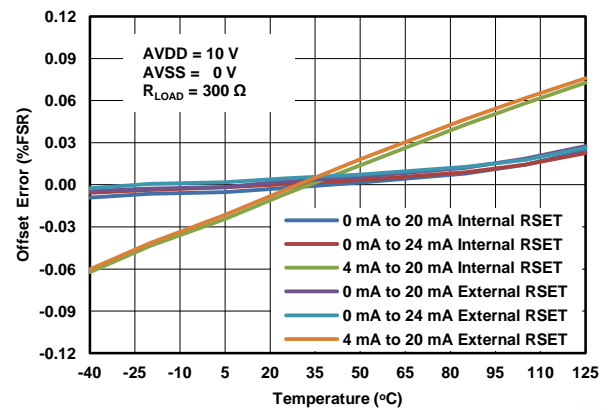


Figure 69. IOUT OFFSET ERROR vs TEMPERATURE



TYPICAL CHARACTERISTICS (continued)

At  $T_A = +25^\circ\text{C}$ , unless otherwise noted.

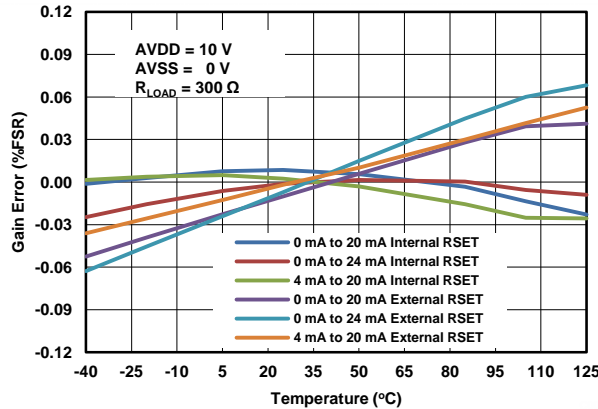


Figure 70. IOUT GAIN ERROR vs TEMPERATURE

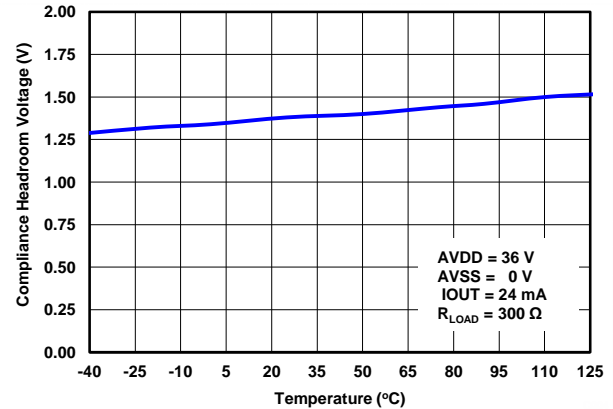


Figure 71. COMPLIANCE HEADROOM VOLTAGE<sup>(1)</sup> vs TEMPERATURE

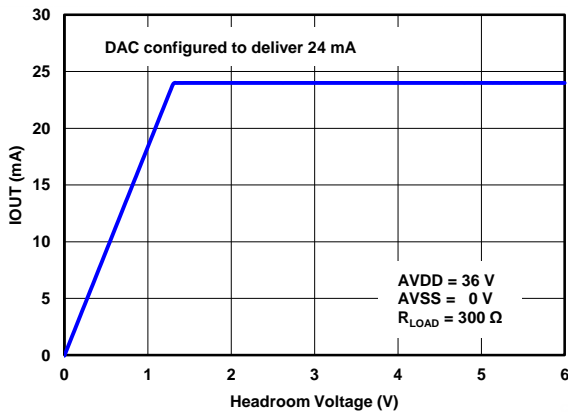


Figure 72. IOUT vs COMPLIANCE HEADROOM VOLTAGE<sup>(1)</sup>

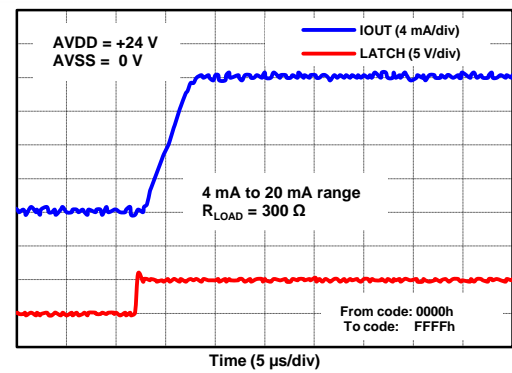


Figure 73. 4 mA to 20 mA RISING

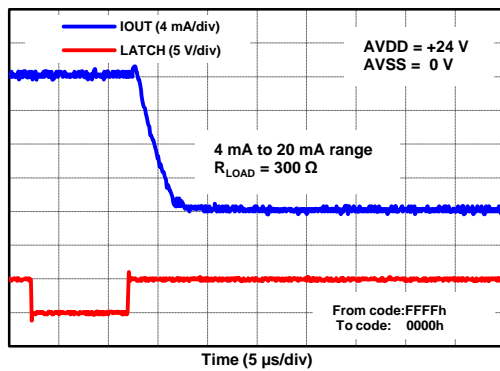


Figure 74. 4 mA to 20 mA FALLING

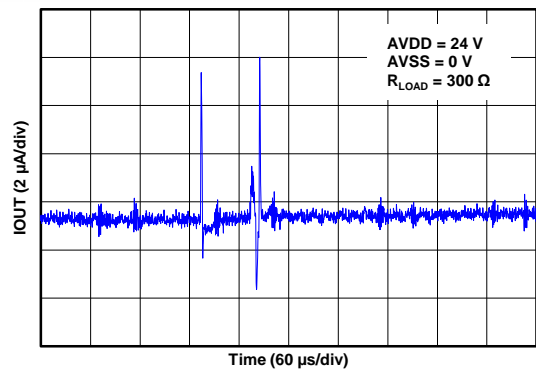


Figure 75. IOUT POWER-ON GLITCH

(1) Compliance voltage headroom is defined as the drop from AVDD pin to the IOUT pin.

TYPICAL CHARACTERISTICS (continued)

At  $T_A = +25^\circ\text{C}$ , unless otherwise noted.

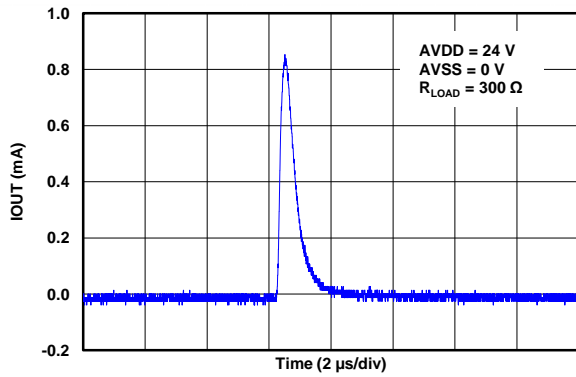


Figure 76. IOUT OUTPUT ENABLE GLITCH

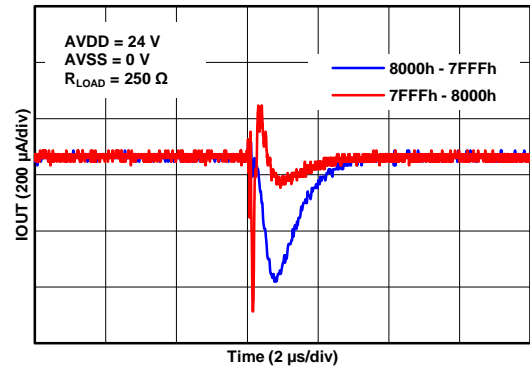


Figure 77. IOUT DIGITAL-TO-ANALOG GLITCH

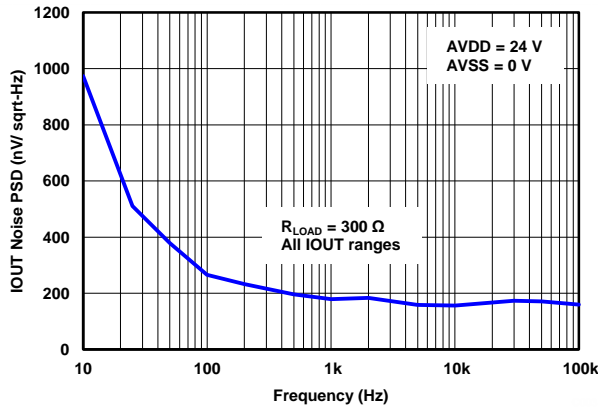


Figure 78. IOUT NOISE PSD vs FREQUENCY

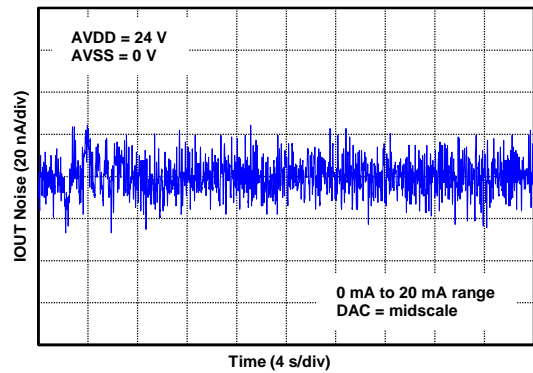


Figure 79. IOUT PEAK-TO-PEAK NOISE vs TIME (0.1 Hz to 10 Hz)

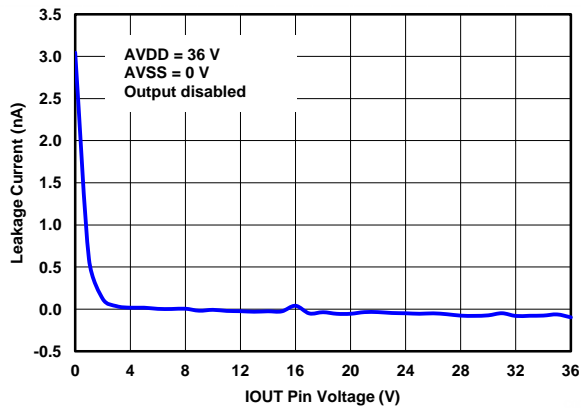


Figure 80. IOUT Hi-Z LEAKAGE CURRENT vs VOLTAGE

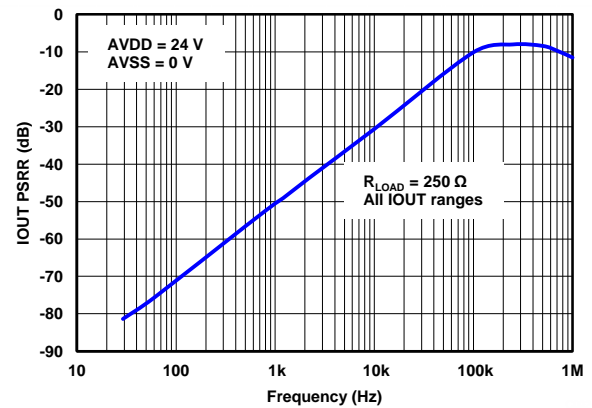


Figure 81. IOUT PSRR vs FREQUENCY

## THEORY OF OPERATION

### DAC ARCHITECTURE

The DAC8760 and DAC7760 (DACx760) consist of a resistor-string digital-to-analog converter (DAC) followed by a buffer amplifier. The output of the buffer drives the current output and the voltage output. The resistor-string section is simply a string of resistors, each of value  $R$ , from REF to GND, as Figure 82 illustrates. This type of architecture makes sure the DAC is monotonic. The 16-bit binary digital code (DAC8760) loaded to the DAC register determines at which node on the string the voltage is tapped off before it is fed into the output amplifier.

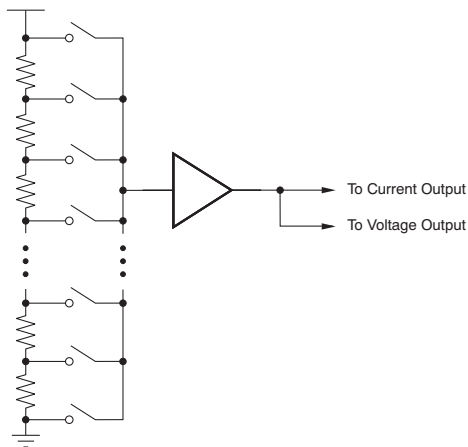


Figure 82. DAC Structure: Resistor String

The current-output stage converts the voltage output from the string to current. The voltage output provides a buffered output of the programmed range to the external load. When the current output or the voltage output is disabled, it is in a high impedance (Hi-Z) state. After power-on, both output stages are disabled. Refer to the [CONTROLLING THE VOUT AND IOUT PINS](#) section for different options to configure the current and voltage output pins.

### VOLTAGE OUTPUT STAGE

The voltage output stage as conceptualized in Figure 83 provides the voltage output according to the DAC code and the output range setting. The output range can be programmed as 0 V to +5 V or 0 V to +10 V for unipolar output mode, and  $\pm 5$  V or  $\pm 10$  V for bipolar output mode. In addition, an option is available to increase the output voltage range by 10%. The output current drive can be up to 10 mA. The output stage has short-circuit current protection that limits the output current to 30 mA. To maintain proper performance, a minimum 0.5-V power-supply headroom is required. The voltage output is able to drive a capacitive load up to 1  $\mu$ F. For loads greater than 20 nF, an external compensation capacitor can be connected between CMP and VOUT to keep the output voltage stable at the expense of reduced bandwidth and increased settling time.

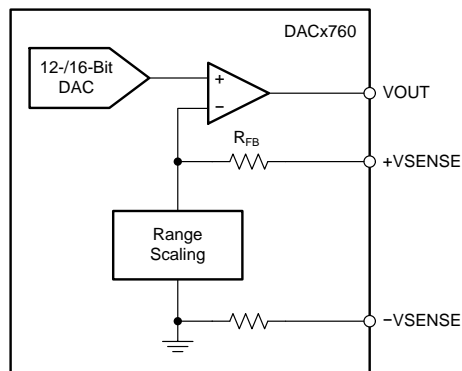


Figure 83. Voltage Output

The +VSENSE pin is provided to enable sensing of the load by connecting to points electrically closer to the load. This configuration allows the internal output amplifier to make sure that the correct voltage is applied across the load, as long as headroom is available on the power supply. Ideally, this pin is used to correct for resistive drops on the system board and is connected to VOUT at the terminals. In some cases, both VOUT and +VSENSE are brought out as terminals and, through separate lines, connected remotely together at the load. In such cases, if the +VSENSE line is cut, the amplifier loop is broken; use an optional 5-kΩ resistor between VOUT and +VSENSE to prevent this from occurring. The –VSENSE pin, on the other hand, is provided as a GND sense reference output from the internal VOUT amplifier. The output swing of the VOUT amplifier is relative to the voltage seen at this pin. The actual voltage difference between the –VSENSE pin and the device GND pins is not expected to be more than a few 100 μV. The internal resistor shown in [Figure 83](#) between the device internal GND and the –VSENSE pin is typically 2 kΩ.

After power on, the power-on-reset circuit makes sure that all registers are at their default values. Therefore, the voltage output buffer is in a Hi-Z state; however, the +VSENSE pin connects to the amplifier inputs through an internal 60-kΩ feedback resistor (R<sub>FB</sub> in [Figure 83](#)). If the VOUT and +VSENSE pins are connected together, the VOUT pin is also connected to the same node through the feedback resistor. This node is protected by internal circuitry and settles to a value between GND and the reference input.

The output voltage (VOUT) can be expressed as [Equation 1](#) and [Equation 2](#).

For unipolar output mode:

$$VOUT = VREF \cdot GAIN \cdot \frac{CODE}{2^N} \tag{1}$$

For bipolar output mode:

$$VOUT = VREF \cdot GAIN \cdot \frac{CODE}{2^N} - GAIN \cdot \frac{VREF}{2}$$

where

- CODE is the decimal equivalent of the code loaded to the DAC.
- N is the bits of resolution; 16 for DAC8760 and 12 for DAC7760.
- VREF is the reference voltage; for internal reference, VREF = +5.0 V.
- GAIN is automatically selected for a desired voltage output range as shown in [Table 1](#). (2)

**Table 1. Voltage Output Range vs Gain Setting<sup>(1)</sup>**

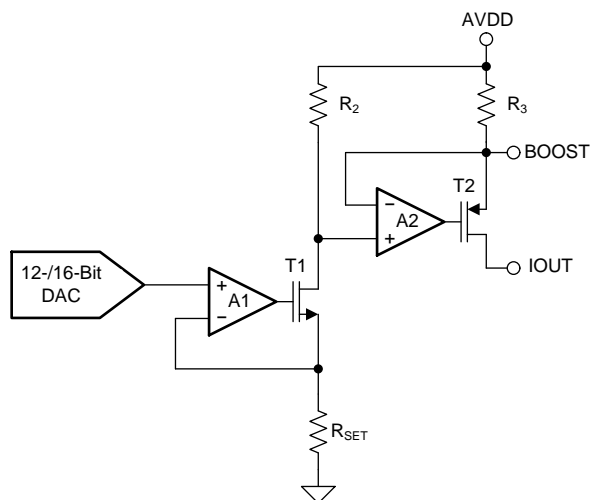
VOLTAGE OUTPUT RANGE	GAIN
0 V to +5 V	1
0 V to +10 V	2
±5 V	2
±10 V	4

(1) VREF = +5.0 V

The voltage range is set according to the value of the RANGE bits and the OVR bit in the [Control Register](#). The OVR bit makes the gain value in [Table 1](#) increase by 10%, thereby increasing the voltage output range, as shown in [Table 15](#). Refer to the [SETTING VOLTAGE AND CURRENT OUTPUT RANGES](#) section for more details.

## CURRENT OUTPUT STAGE

The current output stage consists of a preconditioner and a current source as conceptualized in [Figure 84](#). This stage provides a current output according to the DAC code. The output range can be programmed as 0 mA to 20 mA, 0 mA to 24 mA, or 4 mA to 20 mA. An external boost transistor can be used to reduce the power dissipation of the device. The maximum compliance voltage on pin IOUT equals (AVDD – 2 V). In single power-supply mode, the maximum AVDD is 36 V, and the maximum compliance voltage is 34 V. After power on, the IOUT pin is in a Hi-Z state.



**Figure 84. Current Output**

Resistor  $R_{SET}$  (used to convert the DAC voltage to current) determines the stability of the output current over temperature. If desired, an external, low-drift, precision 15-k $\Omega$  resistor can be connected to the ISET-R pin and used instead of the internal  $R_{SET}$  resistor.

For a 5-V reference, the output can be expressed as shown in [Equation 3](#) through [Equation 5](#).

For a 0-mA to 20-mA output range:

$$I_{OUT} = 20\text{mA} \cdot \frac{CODE}{2^N} \quad (3)$$

For a 0-mA to 24-mA output range:

$$I_{OUT} = 24\text{mA} \cdot \frac{CODE}{2^N} \quad (4)$$

For a 4-mA to 20-mA output range:

$$I_{OUT} = 16\text{mA} \cdot \frac{CODE}{2^N} + 4\text{mA}$$

where

- $CODE$  is the decimal equivalent of the code loaded to the DAC.
- $N$  is the bits of resolution; 16 for DAC8760 and 12 for DAC7760. (5)

The current-output range is normally set according to the value of the RANGE bits in the [Control Register](#). When both the voltage and current outputs are enabled in dual-output mode, the range is set by the IOUT RANGE bits in the [Configuration Register](#). Refer to the [SETTING VOLTAGE AND CURRENT OUTPUT RANGES](#) section for more details. More details on controlling the current output when both the VOUT and IOUT pins are simultaneously enabled are provided in the [Application Information](#) section under [CONTROLLING THE VOUT AND IOUT PINS](#).

## SERIAL PERIPHERAL INTERFACE (SPI)

The device is controlled over a versatile four-wire serial interface (SDI, SDO, SCLK, and LATCH) that operates at clock rates of up to 30 MHz and is compatible with SPI, QSPI™, Microwire, and digital signal processing (DSP) standards. The SPI communication command consists of a write address byte and a data word for a total of 24 bits. The timing for the digital interface is shown in [Figure 1](#), [Figure 2](#), and [Figure 3](#).

### SPI Shift Register

The default frame is 24 bits wide (refer to the [FRAME ERROR CHECKING](#) section for 32-bit frame mode) and begins with the rising edge of SCLK that clocks in the MSB. The subsequent bits are latched on successive rising edges of SCLK. The default 24-bit input frame consists of an 8-bit address byte followed by a 16-bit data word as shown in [Table 2](#).

**Table 2. Default SPI Frame**

BIT 23:BIT 16	BIT 15:BIT 0
Address byte	Data word

The host processor must issue 24 bits before it issues a rising edge on the LATCH pin. Input data bits are clocked in regardless of the LATCH pin and are unconditionally latched on the rising edge of LATCH. By default, the SPI shift register resets to 000000h at power on or after a reset.

### Write Operation

A write operation is accomplished when the address byte is set according to [Table 3](#). For more information on the DACx760 registers, see the [DACx760 COMMANDS AND REGISTER MAP](#) section.

**Table 3. Write Address Functions**

ADDRESS BYTE	FUNCTION
0x00	No operation (NOP)
0x01	Write DAC Data register
0x02	Register read
0x55	Write control register
0x56	Write reset register
0x57	Write configuration register
0x58	Write DAC gain calibration register
0x59	Write DAC zero calibration register
0x95	Watchdog timer reset

### Read Operation

A read operation is accomplished when the address byte is 0x02. Follow the read operation with a no-operation (NOP) command to clock out an addressed register, as shown in [Figure 2](#). To read from a register, the address byte and data word is as shown in [Table 4](#). The read register value is output MSB first on SDO on successive falling edges of SCLK.

**Table 4. Default SPI Frame for Register Read**

ADDRESS BYTE	DATA WORD	
	BIT 15:BIT 6	BIT 5:BIT 0
0x02	X ( <i>don't care</i> )	Register read address (see <a href="#">Table 5</a> )

Table 5 shows the register read addresses available on the DACx760 devices.

**Table 5. Register Read Address Functions**

READ ADDRESS <sup>(1)</sup>	FUNCTION
XX XX00	Read status register
XX XX01	Read DAC data register
XX XX10	Read control register
00 1011	Read configuration register
01 0011	Read DAC gain calibration register
01 0111	Read DAC zero calibration register

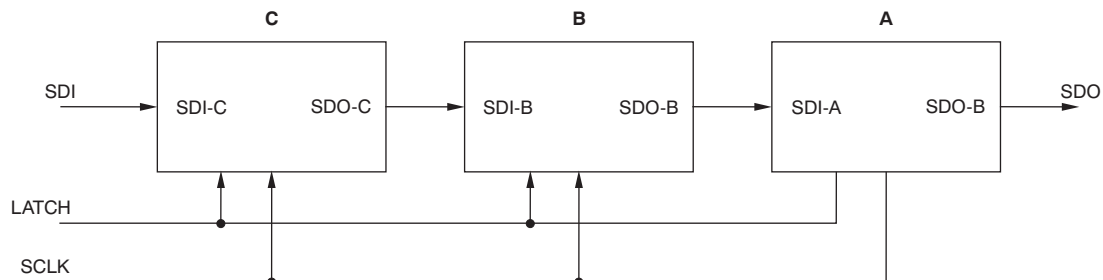
(1) X denotes *don't care* bits.

### Stand-Alone Operation

SCLK can operate in either continuous or burst mode as long as the LATCH rising edge occurs after the appropriate number of SCLK cycles. Providing more than or less than 24 SCLK cycles before the rising edge of LATCH results in incorrect data being programmed into the device registers and incorrect data sent out on SDO. The rising edge of SCLK that clocks in the MSB of the 24-bit input frame marks the beginning of the write cycle, and data are written to the addressed registers on the rising edge of LATCH.

### Daisy-Chain Operation

For systems that contain multiple DACx760s, use the SDO pin to daisy-chain several devices. This mode is useful in reducing the number of serial interface lines in applications that use multiple SPI devices. Daisy-chain mode is enabled by setting the DCEN bit of the control register to '1'. By connecting the SDO of the first device to the SDI input of the next device in the chain, a multiple-device interface is constructed, as Figure 85 illustrates.



**Figure 85. Three DACx760s in Daisy-Chain Mode**

Like stand-alone operation, the SPI daisy-chain write operation requires one frame, and the read requires two frames. The rising edge of SCLK that clocks in the MSB of the input frame marks the beginning of the write cycle. When the serial transfer to all devices is complete, LATCH is taken high. This action transfers the data from the SPI shift registers to the device internal register of each DACx760 in the daisy-chain. However, the number of clocks in each frame in this case depends on the number of devices in the daisy chain. For two devices, each frame is 48 clocks; the first 24 clocks are for the second DAC and the next 24 bits are for the first DAC. For a readback, the data are read from the two DACs in the following 48-bit frame; the first 24 clocks are for the second DAC and the next 24 clocks are for the first DAC. The input data to the DACs during the second frame can be another command or NOP. Similar to the two-device case described, for N devices, each frame is  $N \times 24$  clocks, where N is the total number of DACx760s in the chain.

The serial clock can be a continuous or gated clock. A continuous SCLK source can only be used if LATCH is taken high after the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles must be used and LATCH must be taken high after the final clock to latch the data.

## DACx760 COMMANDS AND REGISTER MAP

Table 6 shows the available commands and registers on the DACx760 devices. *No operation*, *read operation*, and *watchdog timer* refer to commands and are not explicit registers. For more information on these commands, see the [Read Operation](#) and [WATCHDOG TIMER](#) sections. See the [DACx760 Register Descriptions](#) section for descriptions of all DACx760 registers.

**Table 6. Command and Register Map**

REGISTER / COMMAND	READ/WRITE ACCESS	DATA BITS (DB15:DB0)															
		15	14	13	12	11	10:9	8	7	6	5	4	3	2	1	0	
Control	R/W	CLRSEL	OVR	REXT	OUTEN	SRCLK			SRSTEP			SREN	DCEN	RANGE			
Configuration	R/W	X <sup>(1)</sup>				IOUT RANGE	DUAL OUTEN	APD	Reserved	CALEN	HARTEN	CRCCEN	WDEN	WDPD			
DAC Data <sup>(2)</sup>	R/W	D15:D0															
No operation <sup>(3)</sup>	—	X															
Read Operation <sup>(3)</sup>	—	X								READ ADDRESS							
Reset	W																RESET
Status	R	Reserved										CRC-FLT	WD-FLT	I-FLT	SR-ON	T-FLT	
DAC Gain Calibration <sup>(2)</sup>	RW	G15:G0, unsigned															
DAC Zero Calibration <sup>(2)</sup>	RW	Z15:Z0, signed															
WATCHDOG TIMER <sup>(3)</sup>	—	X															

- (1) X denotes *don't care* bits.
- (2) DAC8760 (16-bit version) shown. DAC7760 (12-bit version) contents are located in DB15:DB4. For DAC7760, DB3:DB0 are *don't care* bits when writing and zeros when reading.
- (3) *No operation*, *read operation*, and *watchdog timer* are commands and not registers.

## DACx760 Register Descriptions

### Control Register

The DACx760 control register is written to at address 0x55. Table 7 shows the description for the control register bits.

**Table 7. Control Register**

DATA BIT(S)	NAME	DEFAULT	DESCRIPTION
DB15	CLRSEL	0	VOUT clear value select bit. When bit = '0', VOUT is 0 V in <a href="#">DAC CLEAR</a> mode or after reset. When bit = '1', VOUT is midscale in unipolar output and negative-full-scale in bipolar output in <a href="#">DAC CLEAR</a> mode or after reset.
DB14	OVR	0	Setting the bit increases the voltage output range by 10%.
DB13	REXT	0	External current setting resistor enable.
DB12	OUTEN	0	Output enable. Bit = '1': Output is determined by RANGE bits. Bit = '0': Output is disabled. IOUT and VOUT are <i>Hi-Z</i> .
DB11:DB8	SRCLK[3:0]	0000	Slew rate clock control. Ignored when bit SREN = '0'
DB7:DB5	SRSTEP[2:0]	000	Slew rate step size control. Ignored when bit SREN = '0'
DB4	SREN	0	Slew Rate Enable. Bit = '1': Slew rate control is enabled, and the ramp speed of the output change is determined by SRCLK and SRSTEP. Bit = '0': Slew rate control is disabled. Bits SRCLK and SRSTEP are ignored. The output changes to the new level immediately.
DB3	DCEN	0	Daisy-chain enable.
DB2:DB0	RANGE[2:0]	000	Output range bits.



### Configuration Register

The DACx760 configuration register is written to at address 0x57. [Table 8](#) summarizes the description for the configuration register bits.

**Table 8. Configuration Register**

DATA BIT(S)	NAME	DEFAULT	DESCRIPTION
DB15:DB11		0h	Reserved. User must not write any value other than zero to these bits.
DB10:DB9	IOUT RANGE	00	IOUT range. These bits are only used if both voltage and current outputs are simultaneously enabled via bit 8 (DUAL OUTEN). The voltage output range is still controlled by bits 2:0 of the <a href="#">Control Register</a> (RANGE bits). The current range is controlled by these bits and has similar behavior to RANGE[1:0] when RANGE[2] = '1'. However, unlike the RANGE bits, a change to this field does not make the DAC data register go to its default value.
DB8	DUAL OUTEN	0	DAC dual output enable. This bit controls if the voltage and current outputs are enabled simultaneously. Both are enabled when this bit is high. However, both outputs are controlled by the same DAC data register.
DB7	APD	0	Alternate power down. On power-up, +VSENSE is connected to the internal VOUT amplifier inverting terminal. Diodes exist at this node to REFIN and GND. Setting this bit connects this node to ground through a resistor. When set, the equivalent resistance seen from +VSENSE to GND is 70 kΩ. This is useful in applications where the VOUT and IOUT terminals are tied together.
DB6		0	Reserved. Do not write any value other than zero to these bits.
DB5	CALEN	0	User calibration enable. When user calibration is enabled, the DAC data are adjusted according to the contents of the gain and zero calibration registers. See the <a href="#">USER CALIBRATION</a> section.
DB4	HARTEN	0	Enable interface through HART-IN pin (only valid for IOUT set to 4-mA to 20-mA range via RANGE bits). Bit = '1': HART signal is connected through internal resistor and modulates output current. Bit = '0': HART interface is disabled.
DB3	CRCEN	0	Enable frame error checking.
DB2	WDEN	0	Watchdog timer enable.
DB1:DB0	WDPD[1:0]	00	Watchdog timeout period.

### DAC Registers

The DAC registers consist of a DAC data register ([Table 9](#)), a DAC gain calibration register ([Table 10](#)), and a DAC zero calibration register ([Table 11](#)). User calibration as described in the [USER CALIBRATION](#) section is a feature that allows for trimming the system gain and zero errors. [Table 9](#) through [Table 11](#) show the DAC8760, 16-bit version of these registers. The DAC7760 (12-bit version) register contents are located in DB15:DB4. For DAC7760, DB3:DB0 are *don't care* bits when writing and zeros when reading.

**Table 9. DAC Data Register**

DATA BITS	NAME	DEFAULT	DESCRIPTION
DB15:DB0	D15:D0	0000h	DAC data register. Format is unsigned straight binary.

**Table 10. DAC Gain Calibration Register**

DATA BITS	NAME	DEFAULT	DESCRIPTION
DB15:DB0	G15:G0	0000h	Voltage and current gain calibration register for user calibration. Format is unsigned straight binary.

**Table 11. DAC Zero Calibration Register**

DATA BITS	NAME	DEFAULT	DESCRIPTION
DB15:DB0	Z15:Z0	0000h	Voltage and current zero calibration register for user calibration. Format is two's complement.

### Reset Register

The DACx760 reset register is written to at address 0x56. [Table 12](#) provides the description.

**Table 12. Reset Register**

DATA BIT(S)	NAME	DEFAULT	DESCRIPTION
DB15:DB1		0000h	Reserved. Writing to these bits does not cause any change.
DB0	RESET	0	Software reset bit. Writing 1 to the bit performs a software reset to reset all registers and the $\overline{\text{ALARM}}$ status to the respective power-on reset default value. After reset completes the RESET bit clears itself.

### Status Register

This read-only register consists of four  $\overline{\text{ALARM}}$  status bits (CRC-FLT, WD-FLT, I-FLT, and T-FLT) and bit SR-ON that shows the slew rate status.

The device continuously monitors the output and die temperature. When an alarm occurs, the corresponding  $\overline{\text{ALARM}}$  status bit is set ('1'). Whenever an  $\overline{\text{ALARM}}$  status bit is set, it remains set until the event that caused it is resolved. The  $\overline{\text{ALARM}}$  bit can only be cleared by performing a software reset, or a power-on reset (by cycling power), or having the error condition resolved. These bits are reasserted if the ALARM condition continues to exist in the next monitoring cycle.

The  $\overline{\text{ALARM}}$  bit goes to '0' when the error condition is resolved.

**Table 13. Status Register**

DATA BIT(S)	NAME	DEFAULT	DESCRIPTION
DB15:DB5		000h	Reserved. Reading these bits returns 0.
DB4	CRC-FLT	0	Bit = '1' indicates CRC error on SPI frame. Bit = '0' indicates normal operation.
DB3	WD-FLT	0	Bit = '1' indicates watchdog timer timeout. Bit = '0' indicates normal operation.
DB2	I-FLT	0	Bit = '1' indicates <i>Open Circuit or Compliance Voltage Violation</i> in IOUT loading. Bit = '0' indicates IOUT load is at normal condition.
DB1	SR-ON	0	Bit = '1' when DAC code is slewing as determined by SRCLK and SRSTEP. Bit = '0' when DAC code is not slewing.
DB0	T-FLT	0	Bit = '1' indicates die temperature is over +142°C. Bit = '0' indicates die temperature is not over +142°C.

## SETTING VOLTAGE AND CURRENT OUTPUT RANGES

For voltage and current outputs in normal mode (VOUT and IOUT are not simultaneously enabled), the output range is set according to [Table 14](#).

**Table 14. RANGE Bits vs Output Range**

RANGE	OUTPUT RANGE
000	0 V to +5 V
001	0 V to +10 V
010	±5 V
011	±10 V
100	Not allowed <sup>(1)</sup>
101	4 mA to 20 mA
110	0 mA to 20 mA
111	0 mA to 24 mA

(1) RANGE bits cannot be programmed to 0x100. Previous value is held when this command is written.

Note that changing the RANGE bits at any time causes the DAC data register to be cleared based on the value of CLR-SEL (pin or register bit) and the new value of the RANGE bits.

In addition to the RANGE bits, the OVR bit extends the voltage output range by 10%. if the OVR bit is set, the voltage output range follows [Table 15](#), as long as there is headroom with the supply.

**Table 15. Voltage Output Overrange**

VOLTAGE OUTPUT RANGE	VOLTAGE OUTPUT OVERRANGE
0 V to +5 V	0 V to 5.5 V
0 V to +10 V	0 V to +11 V
±5 V	±5.5 V
±10 V	±11 V

When VOUT and IOUT are simultaneously enabled (dual-output mode) by setting the DUAL OUTEN bit in the [Configuration Register](#), the voltage output is controlled by the RANGE bits in the [Control Register](#) (see [Table 16](#)), and the current output is controlled by the IOUT RANGE bits in the [Configuration Register](#) (see [Table 17](#)).

**Table 16. RANGE Bits versus Voltage Output Range in Dual-Output Mode**

RANGE	OUTPUT RANGE
000	0 V to +5 V
001	0 V to +10 V
010	±5 V
011	±10 V
100	Not allowed <sup>(1)</sup>
1xx	Disabled

(1) RANGE bits cannot be programmed to 0x100. Previous value is held when this command is written.

**Table 17. IOUT RANGE Bits versus Current Output Range in Dual-Output Mode**

RANGE	OUTPUT RANGE
00	Disabled
01	4 mA to 20 mA
10	0 mA to 20 mA
11	0 mA to 24 mA

## INTERNAL REFERENCE

The DACx760 includes an integrated 5-V reference with a buffered output (REFOUT) capable of driving up to 5 mA (source or sink) with an initial accuracy of  $\pm 5$  mV maximum and a temperature drift coefficient of 10 ppm/°C maximum.

## DIGITAL POWER SUPPLY

An internally generated 4.6-V supply capable of driving up to 10 mA can be output on DVDD by leaving the DVD-EN pin unconnected. This supply eases the system power supply design especially when an isolation barrier needs to be crossed to generate the digital supply. It can be used to drive isolation components used for the digital data lines and other miscellaneous components like references and temp sensors. See [Figure 91](#) for an example application. If an external supply is preferred, the DVDD pin (which can be driven up to 5.5 V in this case) can be made into an input by tying DVDD-EN to GND. Refer to the [ELECTRICAL CHARACTERISTICS](#) for detailed specifications.

## DAC CLEAR

The DAC has an asynchronous clear function through the CLR pin which is active-high and allows the voltage output to be cleared to either zero-scale code or midscale code. This action is user-selectable through the CLR-SEL pin or the CLRSEL bit of the [Table 7](#), as [Table 18](#) describes. The CLR-SEL pin and CLRSEL register are ORed together. The current output clears to the bottom of its preprogrammed range. When the CLR signal returns to low, the output remains at the cleared value. The pre-clear value can be restored by pulsing the LATCH signal without clocking any data. A new value cannot be programmed until the CLR pin returns to low. Note that in dual-output mode, the value that the DAC data register is cleared to follows the settings for the voltage output mode.

**Table 18. CLR-SEL Options**

CLR-SEL	OUTPUT VALUE	
	UNIPOLAR OUTPUT RANGE	BIPOLAR OUTPUT RANGE
0	0 V	0 V
1	Midscale	Negative full-scale

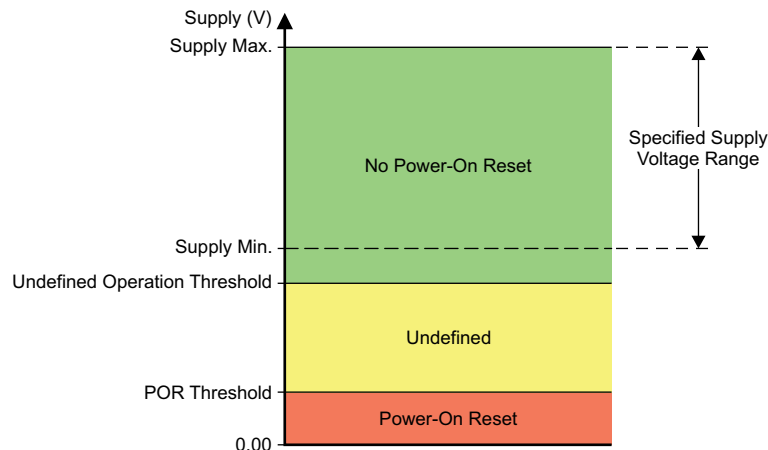
In addition to defining the output value for a clear operation, the CLRSEL bit and the CLR-SEL pin also define the default output value. During the selection of a new voltage range, the output value corresponds to the definitions given in [Table 14](#). To avoid glitches on the output, disable the output by writing a '0' to the OUTEN bit of the [Table 7](#) before changing the voltage range. When the OUTEN bit is set to '1', the output goes to the default value as defined by the CLRSEL bit and the CLR-SEL pin.

## POWER-SUPPLY SEQUENCE

The DACx760 has internal power on reset (POR) circuitry for both the digital DVDD and analog AVDD supplies. This circuitry makes sure that the internal logic and power-on state of the DAC power up to the proper state independent of the supply sequence. While there is no required supply power-on sequence, the recommendation is to first have the digital DVDD supply come up, followed by the analog supplies, AVDD and AVSS. AVSS is powered assuming a negative supply is being used. Otherwise, AVSS is tied to GND.

## POWER-ON RESET

The DACx760 incorporates two internal POR circuits for the DVDD and AVDD supplies. The DVDD and AVDD POR signals are ANDed together so that both supplies must be at their minimal specified values for the device to *not* be in a reset condition. These POR circuits initialize internal logic and registers as well as set the analog outputs to a known state while the device supplies are ramping. All registers are reset to their default values with the default value of the data register being determined by the CLR-SEL pin. The behavior of IOUT and VOUT is described in their respective sections. Typically the POR function can be ignored as long as the device supplies power-up and maintain the specified minimum voltage levels. However, in the case of supply drop or brownout, the DACx760 can have an internal POR reset event or lose digital memory integrity. [Figure 86](#) represents the threshold levels for the internal POR for both the DVDD and AVDD supplies.



**Figure 86. Relevant Voltage Levels for POR Circuit**

For the DVDD supply, no internal POR occurs for nominal supply operation from 2.7 V (supply min) to 5.5 V (supply max). For the DVDD supply region between 2.4 V (undefined operation threshold) and 0.8 V (POR threshold), the internal POR circuit may or may not provide a reset over all temperature conditions. For the DVDD supply below 0.8 V (POR threshold), the internal POR resets as long as the supply voltage is below 0.8 V for approximately 1 ms.

For the AVDD supply, no internal POR occurs for nominal supply operation from 10 V (supply min) to 36 V (supply max). For AVDD supply voltages between 8 V (undefined operation threshold) to 1 V (POR threshold), the internal POR circuit may or may not provide a reset over all temperature conditions. For the AVDD supply below 1 V (POR threshold), the internal POR resets as long as the supply voltage is below 1 V for approximately 1 ms. In case the DVDD or AVDD supply drops to a level where the internal POR signal is indeterminate, either power cycle the device or toggle the LATCH pin followed by a software reset. Both options initialize the internal circuitry to a known state and provide proper operation.

## ALARM DETECTION

The device also provides an alarm detection feature. When one or more of following events occur, the  $\overline{\text{ALARM}}$  pin goes low:

- The current output load is in open circuit; or
- The voltage at IOOUT reaches a level where the accuracy of the output current is compromised. This condition is detected by monitoring internal voltage levels of the IOOUT circuitry and is typically below the specified compliance voltage headroom (defined as the voltage drop between the AVDD and IOOUT pins) minimum of 2 V; or
- The die temperature has exceeded +142°C; or
- The SPI watchdog timer exceeded the timeout period (if enabled); or
- The SPI frame error CRC check encountered an error (if enabled).

When the  $\overline{\text{ALARM}}$  pins of multiple DACx760 devices are connected together to form a wired-AND function, the host processor must read the status register of each device to know all the fault conditions that are present. Note that the thermal alarm has hysteresis of about 18°C. After being set, the alarm only resets when the die temperature drops below +124°C.

## WATCHDOG TIMER

This feature is useful to make sure that communication between the host processor and the DACx760 has not been lost. It can be enabled by setting the WDEN bit of the [Configuration Register](#) to '1'. The watchdog timeout period can be set using the WDPD bits of the configuration register, as shown in [Table 19](#). The timer period is based off an internal oscillator with a typical value of 8 MHz.

**Table 19. Watchdog Timeout Period**

WDPD BITS	WATCHDOG TIMEOUT PERIOD (Typical, ms)
00	10 ms
01	51 ms
10	102 ms
11	204 ms

If enabled, the chip must have an SPI frame with 0x95 as the write address byte written to the device within the programmed timeout period. Otherwise, the ALARM pin asserts low and the WD-FLT bit of the status register is set to '1'. Note that the ALARM pin can be asserted low for any of the different conditions as explained in the [ALARM DETECTION](#) section. The WD-FLT bit is reset to '0' with a software reset, or by disabling the watchdog timer, or by powering down the device.

When using multiple DACx760 devices in a daisy-chain configuration, the open-drain  $\overline{\text{ALARM}}$  pins of all devices can be connected together in a wired-AND function. The watchdog timer can be enabled in any number of the devices in the chain although enabling it in one device is sufficient. The wired-AND  $\overline{\text{ALARM}}$  pin may get pulled low because of the simultaneous presence of different trigger conditions in the daisy-chained devices. The host processor should read the status register of each device to know all the fault conditions present in the chain.

## FRAME ERROR CHECKING

If the DACx760 is used in a noisy environment, error checking can be used to check the integrity of SPI data communication between the device and the host processor. This feature can be enabled by setting the CRCEN bit of the [Configuration Register](#) to '1'. The frame error checking scheme is based on the CRC-8-ATM (HEC) polynomial  $x^8 + x^2 + x + 1$  (that is, 100000111). When error checking is enabled, the SPI frame width is 32 bits, as shown in [Table 20](#). Start with the default 24-bit frame and enable frame error checking through the CRCEN bit and switch to the 32-bit frame. The normal 24-bit SPI data are appended with an 8-bit CRC polynomial by the host processor before feeding it to the device. For a register readback, the CRC polynomial is output on the SDO pins by the device as part of the 32-bit frame.

**Table 20. SPI Frame with Frame Error Checking Enabled**

BIT 31:BIT 8	BIT 7:BIT 0
Normal SPI frame data	8-bit CRC polynomial

The DACx760 decodes the 32-bit input frame data to compute the CRC remainder. If no error exists in the frame, the CRC remainder is zero. When the remainder is non-zero (that is, the input frame has single- or multiple-bit errors), the  $\overline{\text{ALARM}}$  pin asserts low and the CRC-FLT bit of the status register is also set to 1. Note that the  $\overline{\text{ALARM}}$  pin can be asserted low for any of the different conditions as explained in the [ALARM DETECTION](#) section. The CRC-FLT bit is reset to 0 with a software reset, or by disabling the frame error checking, or by powering down the device. In the case of a CRC error, the specific SPI frame is blocked from writing to the device.

Frame error checking can be enabled for any number of DACx760 devices connected in a daisy-chain configuration. However, it is recommended to enable error checking for none or all devices in the chain. When connecting the  $\overline{\text{ALARM}}$  pins of all combined devices, forming a wired-AND function, the host processor should read the status register of each device to know all the fault conditions present in the chain. For proper operation, the host processor must provide the correct number of SCLK cycles in each frame, taking care to identify whether or not error checking is enabled in each device in the daisy-chain.

## USER CALIBRATION

The device implements a user-calibration function to allow for trimming the system gain and zero errors. There is a gain calibration register and a zero calibration register; the DAC output is calibrated according to the value of these registers. The range of gain adjustment is typically  $\pm 50\%$  of full-scale with 1 LSB per step. The gain register must be programmed to a value of 0x8000 to achieve the default gain of 1 because the power-on value of the register is 0x0000, which is equivalent to a gain of 0.5. The zero code adjustment is typically  $\pm 32,768$  LSBs with 1 LSB per step. The input data format of the gain register is unsigned straight binary, and the input data format of the zero register is twos complement. The gain and offset calibration is described by [Equation 6](#)

$$\text{CODE\_OUT} = \text{CODE} \cdot \frac{\text{User\_GAIN} + 2^{15}}{2^{16}} + \text{User\_ZERO}$$

where

- *CODE* is the decimal equivalent of the code loaded to the DAC data register at address 0x01.
- *N* is the bits of resolution; 16 for DAC8760 and 12 for DAC7760.
- *User\_ZERO* is the signed 16-bit code in the zero register.
- *User\_GAIN* is the unsigned 16-bit code in the gain register.
- *CODE\_OUT* is the decimal equivalent of the code loaded to the DAC (limited between 0x0000 to 0xFFFF for DAC8760 and 0x000 to 0xFFF for DAC7760). (6)

This is a purely digital implementation and the output is still limited by the programmed value at both ends of the voltage or current output range. In addition, remember that the correction only makes sense for endpoints inside of the true device end points. To correct more than just the actual device error, for example a system offset, the valid range for the adjustment changes accordingly and must be taken into account. This range is set by the RANGE, OVR, DUAL OUTEN, and IOUT RANGE bits, as described in the [SETTING VOLTAGE AND CURRENT OUTPUT RANGES](#) section

## PROGRAMMABLE SLEW RATE

The slew rate control feature controls the rate at which the output voltage or current changes. With the slew rate control feature disabled, the output changes smoothly at a rate limited by the output drive circuitry and the attached load.

To reduce the slew rate, enable the slew rate control feature through bit 4 of the [Table 7](#). With this feature enabled, the output does not slew directly between the two values. Instead, the output steps digitally at a rate defined by bits [7:5] (SRSTEP) and bits [11:8] (SRCLK) of the control register. SRCLK defines the rate at which the digital slew updates; SRSTEP defines the amount by which the output value changes at each update. If the DAC data register is read while the DAC output is still changing, the instantaneous value is read. [Table 21](#) lists the slew rate step-size options. [Table 22](#) summarizes the slew rate update clock options.

**Table 21. Slew Rate Step-Size (SRSTEP) Options**

SRSTEP	STEP SIZE (LSB)	
	DAC7760	DAC8760
000	0.0625	1
001	0.125	2
010	0.125	4
011	0.5	8
100	1	16
101	2	32
110	4	64
111	8	128



**Table 22. Slew Rate Update Clock (SRCLK) Options**

SRCLK	DAC UPDATE FREQUENCY (Hz)
0000	258,065
0001	200,000
0010	153,845
0011	131,145
0100	115,940
0101	69,565
0110	37,560
0111	25,805
1000	20,150
1001	16,030
1010	10,295
1011	8,280
1100	6,900
1101	5,530
1110	4,240
1111	3,300

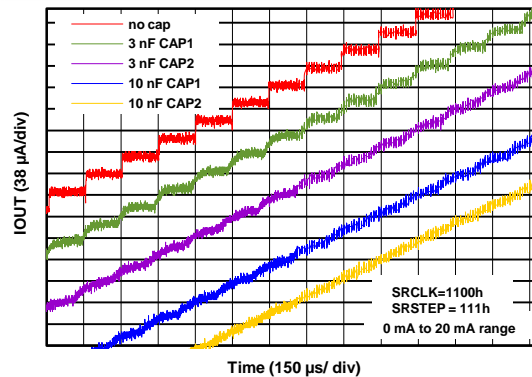
The time required for the output to slew over a given range can be expressed as [Equation 7](#):

$$\text{Slew Time} = \frac{\text{Output Change}}{\text{Step Size} \cdot \text{Update Clock Frequency} \cdot \text{LSB Size}}$$

where

- *Slew Time* is expressed in seconds
  - *Output Change* is expressed in amps (A) for IOOUT or volts (V) for VOUT
- (7)

When the slew rate control feature is enabled, all output changes happen at the programmed slew rate. This configuration results in a staircase formation at the output. If the CLR pin is asserted, the output slews to the zero-scale value at the programmed slew rate. Bit 1 (SR-ON) of the [Status Register](#) can be read to verify that the slew operation has completed. The update clock frequency for any given value is the same for all output ranges. The step size, however, varies across output ranges for a given value of step size because the LSB size is different for each output range. [Figure 87](#) shows an example of IOOUT slewing at a rate set by the above described parameters. In this example for the DAC8760 (LSB size of 305 nA for the 0-mA to 20-mA range), the settings correspond to an update clock frequency of 6.9 kHz and a step size of 128 LSB. As can be seen for the case with no capacitors on CAP1 or CAP2, the steps occur at the update clock frequency (6.9 kHz corresponds to a period close to 150 μs) and the size of each step is about 38 μA (128 × 305 nA). The slew time for a specific code change can be calculated using [Equation 7](#).



**Figure 87. IOOUT vs Time with Digital Slew Rate Control**



## BOOST CONFIGURATION FOR IOOUT

An external NPN transistor can be used as shown in Figure 88 to reduce power dissipation on the die. Most of the load current flows through the NPN transistor with a small amount flowing through the on-chip PMOS transistor based on the gain of the NPN transistor. This reduces the temperature induced drift on the die and internal reference and is an option for use cases at the extreme end of the supply, load current, and ambient temperature ranges. Resistor  $R_2$  stabilizes this circuit for cases where the  $R_{LOAD}$  is a short or a very small load like a multimeter. Recommended values for  $R_1$ ,  $R_2$  and  $C_1$  in this circuit are 1 k $\Omega$ , 20  $\Omega$  and 0.22  $\mu$ F. An equivalent solution is to place  $R_2$  (with a recommended value of 2 k $\Omega$  instead of the 20  $\Omega$ ) in series with the base of the transistor instead of the configuration shown in Figure 88. Note that there is some gain error introduced by this configuration as seen in Figure 47 for the 0-24 mA range. It is recommended that the internal transistor be used in most cases as the values in the ELECTRICAL CHARACTERISTICS are based on the configuration with the internal on chip PMOS transistor.

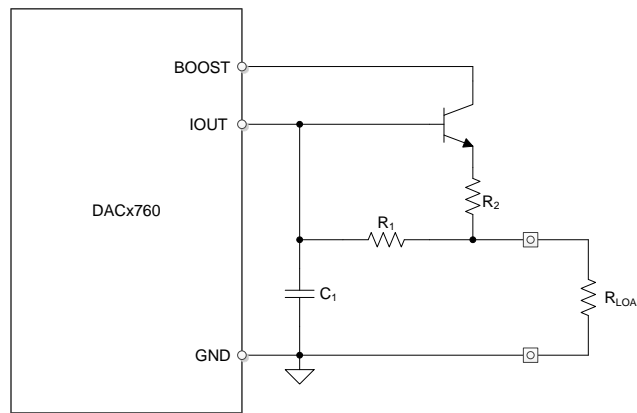


Figure 88. Boost Mode Configuration

## FILTERING THE CURRENT OUTPUT (only on the QFN package)

The QFN package provides access to internal nodes of the circuit as shown in Figure 94. Capacitors can be placed on these pins and AVDD to form a filter on the output current, reducing bandwidth and the slew rate of the output. However, to achieve large reductions in slew rate, the programmable slew rate can be used to avoid having to use large capacitors. Even in that case, the capacitors on CAP1 and CAP2 can be used to smooth out the stairsteps caused by the digital code changes as shown in Figure 89. However, note that power supply ripple will also couple into the part through these capacitors.

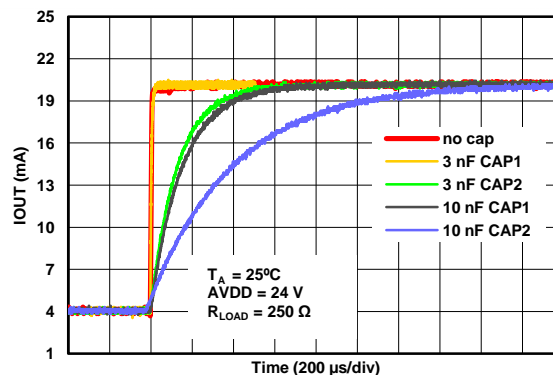


Figure 89. IOOUT vs Time for Different Cap Values on CAP1 and CAP2

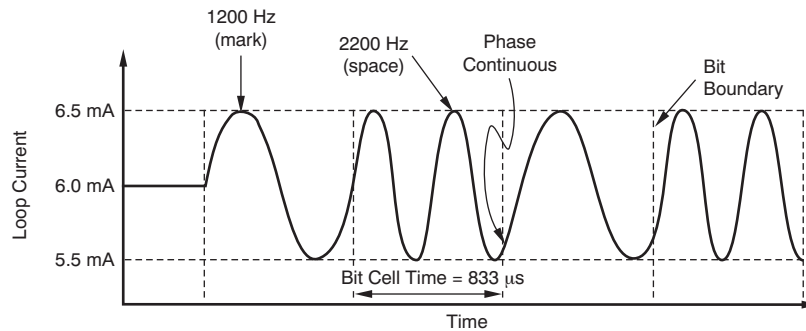
## HART INTERFACE

On the DACx760, HART digital communication can be modulated onto the input signal by two methods:

### For 4-mA to 20-mA Mode

This method is limited to the case where the RANGE bits of the [Table 7](#) are programmed to the 4-mA to 20-mA range. Some applications require going beyond the 4-20 mA range. In those cases, refer to the second method described in this section.

The external HART signal (ac voltage; 500 mV<sub>PP</sub>, 1200 Hz and 2200 Hz) can be capacitively coupled in through the HART-IN pin and transferred to a current that is superimposed on the 4-mA to 20-mA current output. The HART-IN pin has a typical input impedance of 35 kΩ that together with the input capacitor used to couple the external HART signal forms a filter to attenuate frequencies beyond the HART band-pass region. In addition to this filter, an external passive filter is recommended to complete the filtering requirements of the HART specifications. [Figure 90](#) illustrates the output current versus time operation for a typical HART signal.



Note: DC current = 6 mA.

**Figure 90. Output Current vs Time**

[Table 23](#) specifies the performance of the HART-IN pin.

**Table 23. HART-IN Pin Characteristics**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input impedance	HART signal ac-coupled into pin		35		kΩ
Output current (peak-to-peak)	Input signal of 500 mV (peak-to-peak)	0.9	1	1.1	mA

### For All Current Output Modes

The use of the HART-IN pin to implement HART modulation is limited to the case where the RANGE bits of the [Table 7](#) are set to the 4-mA to 20-mA range. To implement HART in all current-output modes, refer to [IMPLEMENTING HART IN ALL CURRENT OUTPUT MODES](#) in the *Application Information* section.

## APPLICATION INFORMATION

### ANALOG OUTPUT (AO) MODULE FOR PLC- AND DCS-BASED CONTROL SYSTEMS IN INDUSTRIAL AUTOMATION AND PROCESS CONTROL

Analog I/O modules are used by programmable logic controllers (PLCs) and distributed control systems (DCSs) to interface to sensors, actuators and other field instruments. These modules must meet stringent electrical specifications for both performance as well as protection. Analog output modules are used to drive actuators and other field elements as part of the overall control system. These outputs are typically current output loops based on the 4-mA to 20-mA range or voltage outputs ranging from 0 V to 5 V, 0 V to 10 V,  $\pm 5$  V, and  $\pm 10$  V. The DACx760 family is an excellent choice for these use cases. Figure 91 illustrates a circuit design for such an application.

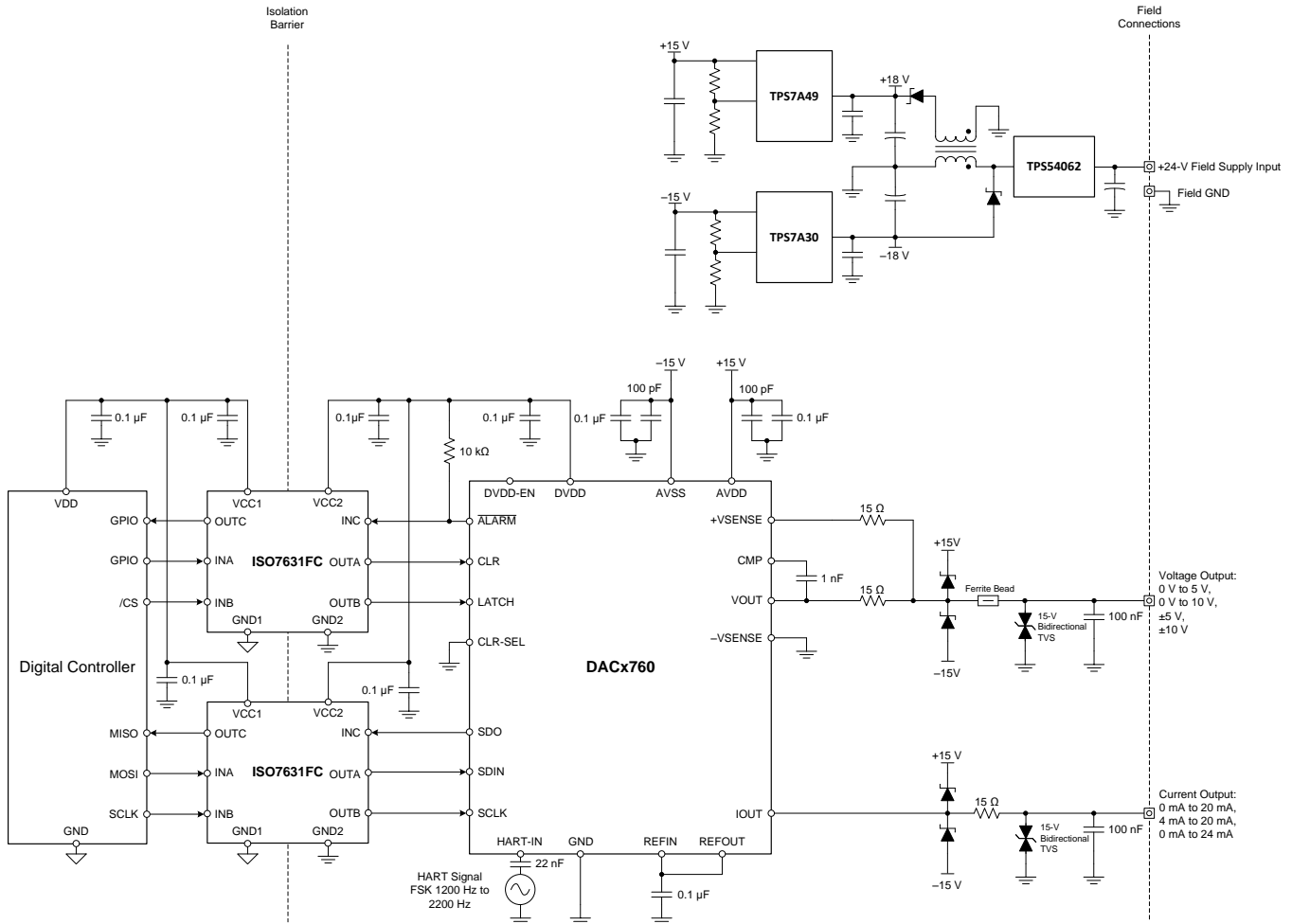


Figure 91. DACx760 in an Analog Output (AO) Module

This circuit generates a clean  $\pm 15$ -V supply using a synchronous step-down regulator (TPS54062) and two high-voltage, ultralow-noise, linear regulators (TPS7A49 and TPS7A30). A field supply terminal is shown instead of the more common use case of a backplane supply. The design uses two triple channel isolators (ISO7631FC) to provide galvanic isolation for the digital lines to communicate to the main controller. Note that these isolators can be driven by the internally-generated supply (DVDD) from the DACx760 to save components and cost. The DACx760 supplies up to 10 mA that meets the supply requirements of the two isolators running at up to 10 Mbps. Note that additional cost savings are possible if noncritical signals such as CLR and  $\overline{\text{ALARM}}$  are tied to GND or left unconnected. Finally, a protection scheme with transient voltage suppressors and other components is placed on all pins which connect to the field devices. In some cases, the protection scheme can be fairly complex involving passive filters and other protection components.

## CONTROLLING THE VOUT AND IOUT PINS

This section describes how to control the VOUT and IOUT pins for three use cases:

### VOUT and IOUT Pins are Independent Outputs, Never Simultaneously Enabled

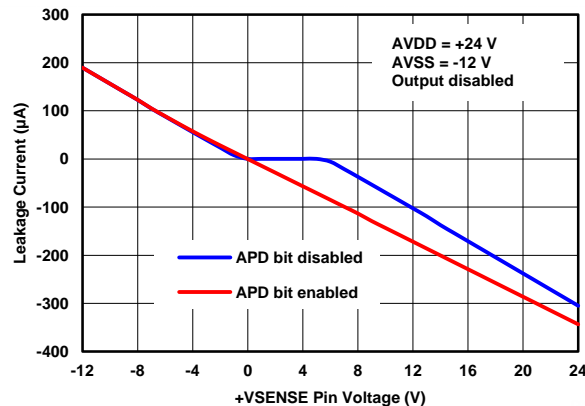
In most applications, VOUT and IOUT are not connected together. In addition, only one is enabled at a time or they are both powered down. In this configuration, bits 10 down to 7 of the [Configuration Register](#) must be set to 0000 (default value). Bits 2 down to 0 of the [Control Register](#) (RANGE bits) control VOUT and IOUT.

### VOUT and IOUT Pins are Independent Outputs, Simultaneously Enabled

When VOUT and IOUT are independent outputs and simultaneously enabled, bit 8 of the [Configuration Register](#) (DUAL OUTEN) must be set to 1. Bits 2 down to 0 of the [Control Register](#) (RANGE bits) control VOUT and bits 10 down to 9 of the [Configuration Register](#) (IOUT RANGE) control IOUT. Note that only one DAC code register exists and therefore the voltage and current outputs are controlled by the same code. Note that changing the RANGE bits at any time will cause the DAC data register to be cleared based on the value of the CLR-SEL pin or CLRSEL register bit and the new value of the RANGE bits.

### VOUT and IOUT Pins are Tied Together, Never Simultaneously Enabled

When the VOUT and IOUT pins are tied together, bit 8 of the [Configuration Register](#) (DUAL OUTEN) must be set to 0. Bits 2 down to 0 of the [Control Register](#) (RANGE) control VOUT and IOUT. Special consideration must be paid to the +VSENSE pin in this case. When VOUT is disabled, the +VSENSE pin is connected to the internal amplifier input through an internal 60-k $\Omega$  resistor as shown in [Figure 83](#). This internal node has diode clamps to REFIN and GND. Setting bit 6 of the [Configuration Register](#) (APD) forces this internal node to be tied to GND via a 10-k $\Omega$  resistor - in effect, the +VSENSE pin is tied to GND via a 70-k $\Omega$  power-down resistor. [Figure 92](#) shows the leakage current into the +VSENSE pin for both settings of the APD bit.



**Figure 92. +VSENSE Leakage Current vs Pin Voltage**

Whether the APD bit is set or not set, the current output in this case incurs a gain error since the internal resistor acts as a parallel load in addition to the external load. If this gain error is undesirable, it can be corrected through the gain calibration register shown in [Table 10](#). Another option is to use the application circuit in [Figure 93](#).

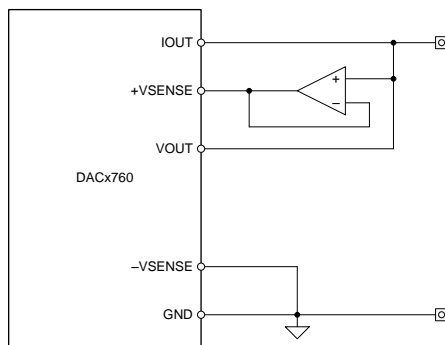


Figure 93. VOUT and IOUT Tied Together to One Terminal

The buffer amplifier prevents leakage through the internal 60-k $\Omega$  resistor in current output mode and does not allow it to be seen as a parallel load. The VOUT pin is in high impedance mode in this case and will allow minimal leakage current. Note that the offset of the external amplifier will add to the overall VOUT offset error and any potential phase shift from the external amplifier can cause VOUT stability issues.

### IMPLEMENTING HART IN ALL CURRENT OUTPUT MODES

If it is desirable to implement HART irrespective of the RANGE bit settings, there are two ways to do this.

#### Using CAP2 Pin on QFN Package

The first method of implementing HART is to couple the signal through the CAP2 pin, as conceptualized in Figure 94. Note that this pin is only available in the QFN-40 package.

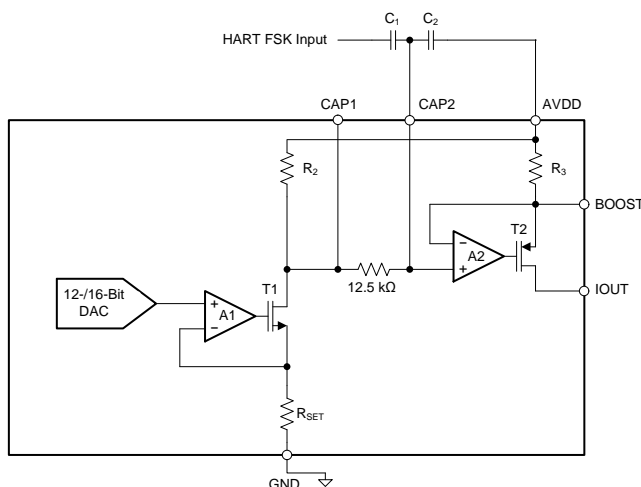


Figure 94. Implementing HART on IOUT Using the CAP2 Pin

In Figure 94,  $R_3$  is nominally 40  $\Omega$ , and  $R_2$  is dependent on the current output range (set by the RANGE bits) as described below:

- 4-mA to 20-mA range:  $R_2 = 2.4$  k $\Omega$  typical
- 0-mA to 20-mA range:  $R_2 = 3$  k $\Omega$  typical
- 0-mA to 24-mA range:  $R_2 = 3.6$  k $\Omega$  typical

The purpose of the 12.5-k $\Omega$  resistor is to create a filter when CAP1 and CAP2 are used.

To insert the external HART signal on the CAP2 pin, an external ac coupling cap is typically connected to CAP2. The high pass filter 3-dB frequency would be determined by the resistive impedance looking into CAP2 ( $R_2 + 12.5$  k $\Omega$ ) and the coupling cap value. The 3-dB frequency would be  $1 / (2 \times \pi \times [R_2 + 12.5 \text{ k}\Omega] \times [\text{Coupling Cap Value}])$ .

After the input HART frequency is greater than the 3-dB frequency, the ac signal is seen at the plus input of amplifier A2 and would therefore be seen across the 40-Ω resistor. To generate a 1-mA signal on the output would therefore require a 40-mV peak-to-peak signal on CAP2. Because most HART modems do not output a 40-mV signal, a capacitive divider is used in the above circuit to attenuate the FSK signal from the modem. In the above circuit, the high pass cutoff frequency would be  $1 / (2 \times \pi \times [R_2 + 12.5 \text{ k}\Omega] \times [C_1 + C_2])$ . There is one disadvantage of this approach: if the AVDD supply was not clean, any ripple on it could couple into the part.

### Using the ISET-R Pin

The second method to implement HART is to couple the HART signal through the ISET-R pin when IOU<sub>T</sub> is operated using an external R<sub>SET</sub> resistor. The FSK signal from the modem is ac coupled into the pin through a series combination of R<sub>in</sub> and C<sub>in</sub> as shown in Figure 95

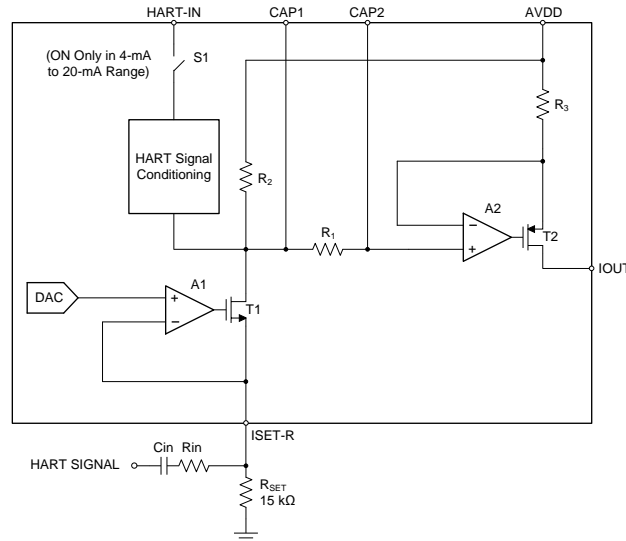


Figure 95. Implementing HART with the ISET-R pin

The magnitude of the ac current output is calculated as  $(V_{\text{HART}} \times k) / R_{\text{in}}$ , where k is a constant that represents the gain transfer function from the ISET-R pin to the IOU<sub>T</sub> pin and depends on the selected current output range as follows: k = 60 for 4-mA to 20-mA range, 75 for 0-mA to 20-mA range, and 90 for 0-mA to 24-mA range. The series input resistor and capacitor form a high-pass filter at the ISET-R pin and C<sub>in</sub> should be selected to make sure that all signals in the HART extended-frequency band pass through unattenuated.

### SHORT-CIRCUIT CURRENT LIMITING

The DACx760 voltage output includes an internal circuit to typically regulate the load current to about 30 mA. However, this parameter is not production tested or trimmed. Optionally, users can use an external current limiting circuit on VOUT. However, if the VOUT, IOU<sub>T</sub> and +VSENSE pins are tied together, this circuit must be placed in the VOUT path before it is tied together to the other pins at the common terminal. The nature of the current-limiting circuit depends on the application and load. An example of a unidirectional current limiter is shown in Figure 96.

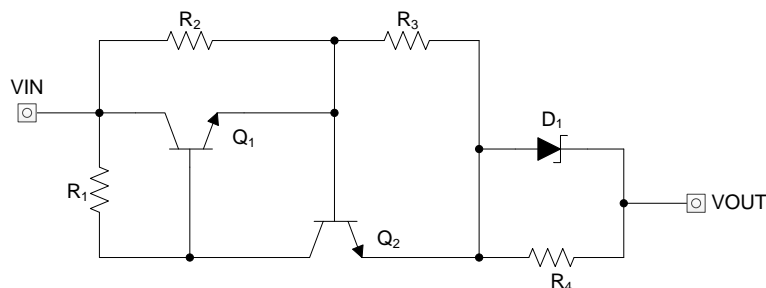


Figure 96. Unidirectional Current Limiter Circuit

Under normal operation, most current in this circuit will flow through  $R_2$  and into  $R_3$ . As current increases through  $R_3$ , so does the voltage drop across  $R_3$ , which increases the base-emitter voltage of  $Q_2$ . Eventually the base-emitter voltage of  $Q_2$  become high enough to turn on  $Q_2$  which will turn off  $Q_1$  and reduce the current that can pass from  $V_{IN}$  to  $V_{OUT}$ . The value of  $R_3$  sets the current limit. Note that this is a very simple example and only applies for sourcing current into a resistive load. For cases involving both sourcing and sinking current as well as nonresistive loads, more complex circuits would be needed to achieve bidirectional current limiting.

## THERMAL CONSIDERATIONS

The DACx760 is designed for a maximum junction temperature of +150°C. In cases where the maximum AVDD is driving maximum current into ground, this could be exceeded. Use the following equation, from the [ABSOLUTE MAXIMUM RATINGS](#), to determine the maximum junction temperature that can be reached:

$$\text{Power Dissipation} = (T_{J_{\max}} - T_A) / \theta_{JA},$$

where  $T_{J_{\max}} = +150^\circ\text{C}$ ,  $T_A$  is the ambient temperature and  $\theta_{JA}$  is the package dependent junction-to-ambient thermal resistance, which is found in the [THERMAL INFORMATION](#) section.

The power dissipation can be calculated by multiplying all the supply voltages with the currents supplied, which is found in the *Power Requirements* subsection of [ELECTRICAL CHARACTERISTICS](#).

Consider an example: IOUT is enabled, supplying 24 mA into GND with a 25°C ambient temperature, AVDD of 24 V, AVSS is tied to GND and DVDD is generated internally. From the specifications table, the max value of AIDD = 3 mA when IOUT is enabled and DAC code = 0x0000. Also, the max value of DIDD = 1 mA. Accordingly, the worst case power dissipation is  $24\text{ V} \times (24\text{ mA} + 3\text{ mA} + 1\text{ mA}) = 672\text{ mW}$ . Using the  $\theta_{JA}$  value for the TSSOP package, we get  $T_{J_{\max}} = +25^\circ\text{C} + (32.3 \times 0.672)^\circ\text{C} = +46.7^\circ\text{C}$ . At +85°C ambient temperature, the corresponding value of  $T_{J_{\max}}$  is +106.7°C. Using this type of analysis, the system designer can both specify and design for the equipment operating conditions. Note that the thermal pad in both packages is recommended to be connected to a copper plane for enhanced thermal performance.

## LAYOUT CONSIDERATIONS

To maximize the performance of the DACx760 in any application, good layout practices and proper circuit design must be followed. A few recommendations specific to the DACx760 are:

1. As is seen in [Figure 94](#), CAP2 is directly connected to the input of the final IOUT amplifier. Any noise or unwanted ac signal routed near the CAP1 and/or CAP2 pins could capacitively couple onto internal nodes and affect IOUT. Therefore, with the QFN package, it is important to avoid routing any digital or HART signal trace over the CAP1 and CAP2 traces.
2. The thermal PAD must be connected to the lowest potential in the system.
3. The +VSENSE connection should be a low-impedance trace connected close to the point of load.
4. AVDD and AVSS should have decoupling capacitors local to the respective pins.
5. The reference capacitor should be placed close to the reference input pin.
6. Avoid routing switching signals near the reference input.
7. For designs that include protection circuits:
  - (a) Place diversion elements, such as TVS diodes or capacitors, close to off-board connectors to make sure that return current from high-energy transients does not cause damage to sensitive devices.
  - (b) Use large, wide traces to provide a low-impedance path to divert high-energy transients away from I/O terminals.

## REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (June 2013) to Revision A	Page
• Changed data sheet from product preview to production data .....	1



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC7760IPWP	ACTIVE	HTSSOP	PWP	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC7760	<a href="#">Samples</a>
DAC7760IPWPR	ACTIVE	HTSSOP	PWP	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC7760	<a href="#">Samples</a>
DAC7760IRHAR	PREVIEW	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-3-260C-168 HR	-40 to 125	DAC7760	
DAC7760IRHAT	PREVIEW	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-3-260C-168 HR	-40 to 125	DAC7760	
DAC8760IPWP	ACTIVE	HTSSOP	PWP	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC8760	<a href="#">Samples</a>
DAC8760IPWPR	ACTIVE	HTSSOP	PWP	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC8760	<a href="#">Samples</a>
DAC8760IRHAR	PREVIEW	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-3-260C-168 HR	-40 to 125	DAC8760	
DAC8760IRHAT	PREVIEW	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-3-260C-168 HR	-40 to 125	DAC8760	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC7760IPWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
DAC8760IPWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

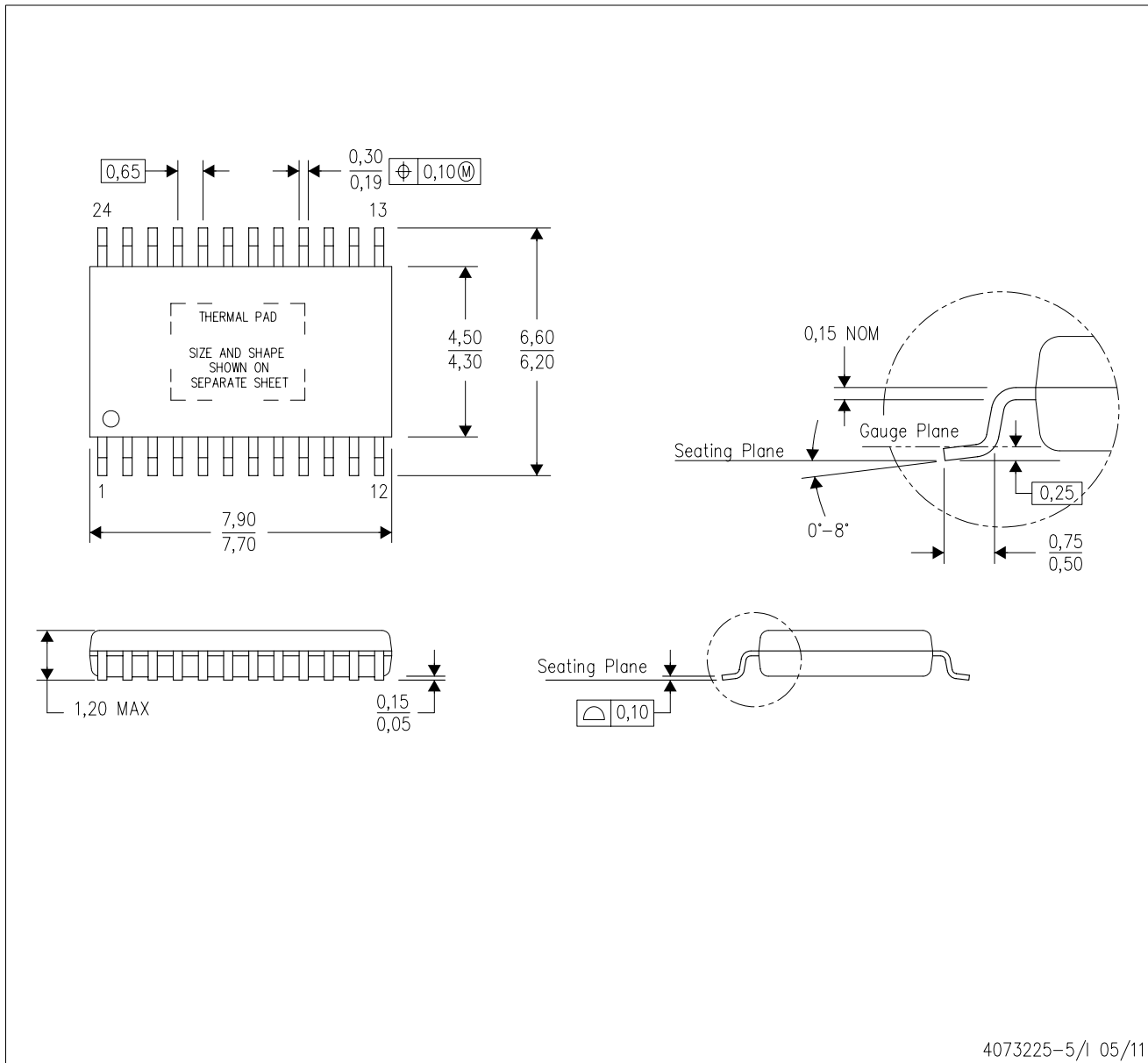

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC7760IPWPR	HTSSOP	PWP	24	2000	367.0	367.0	38.0
DAC8760IPWPR	HTSSOP	PWP	24	2000	367.0	367.0	38.0

# MECHANICAL DATA

PWP (R-PDSO-G24)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

# THERMAL PAD MECHANICAL DATA

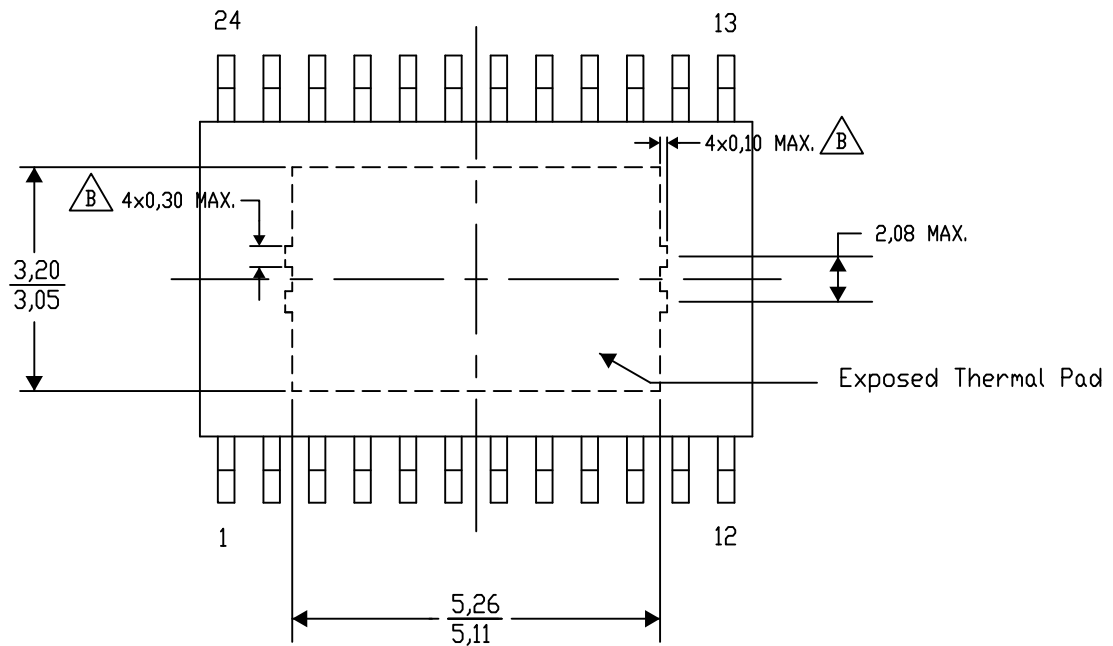
## PWP (R-PDSO-G24) PowerPAD™ SMALL PLASTIC OUTLINE

### THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



4206332-46/AH 11/13

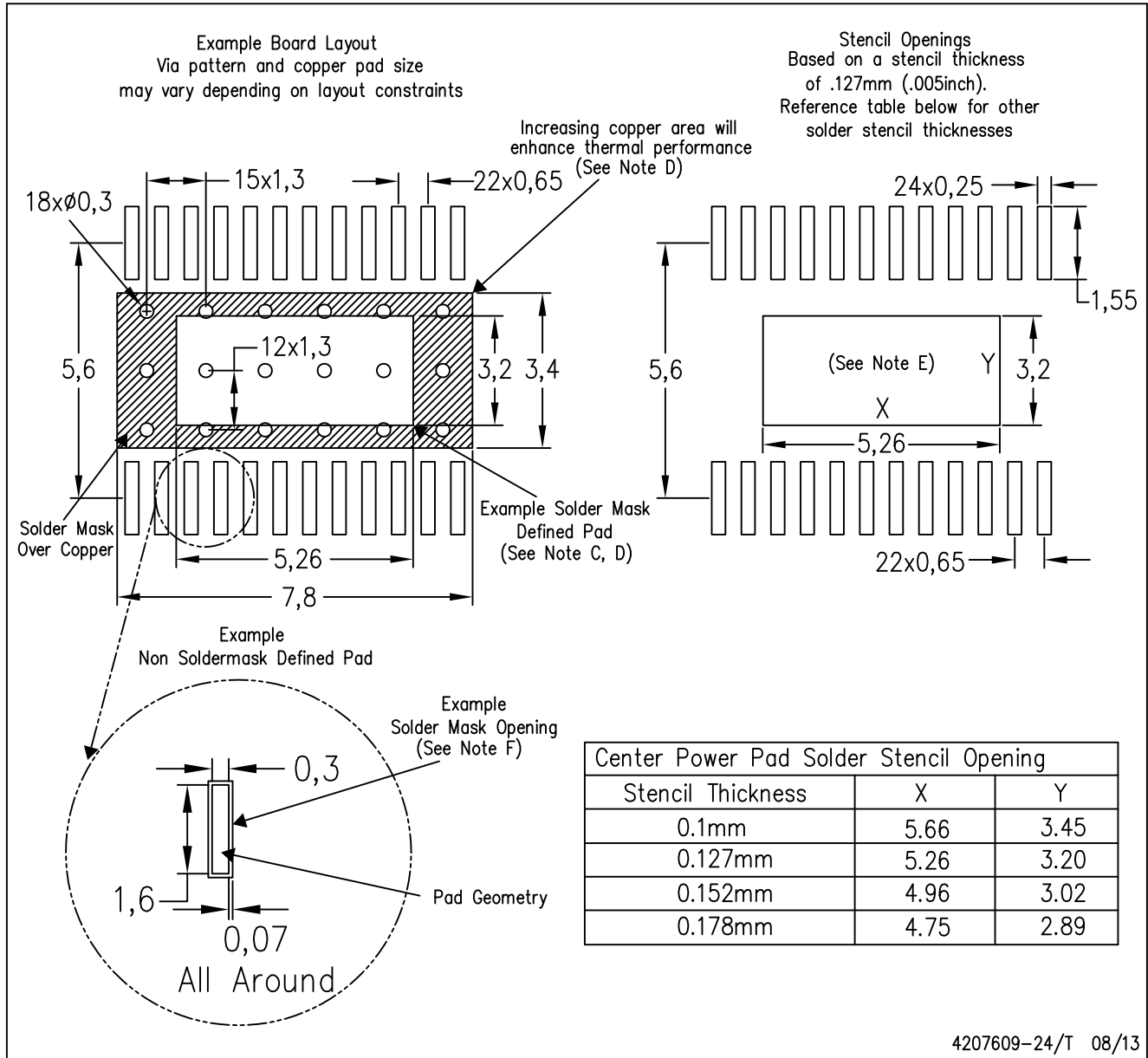
NOTE: A. All linear dimensions are in millimeters

 B. Exposed tie strap features may not be present.

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PWP (R-PDSO-G24)

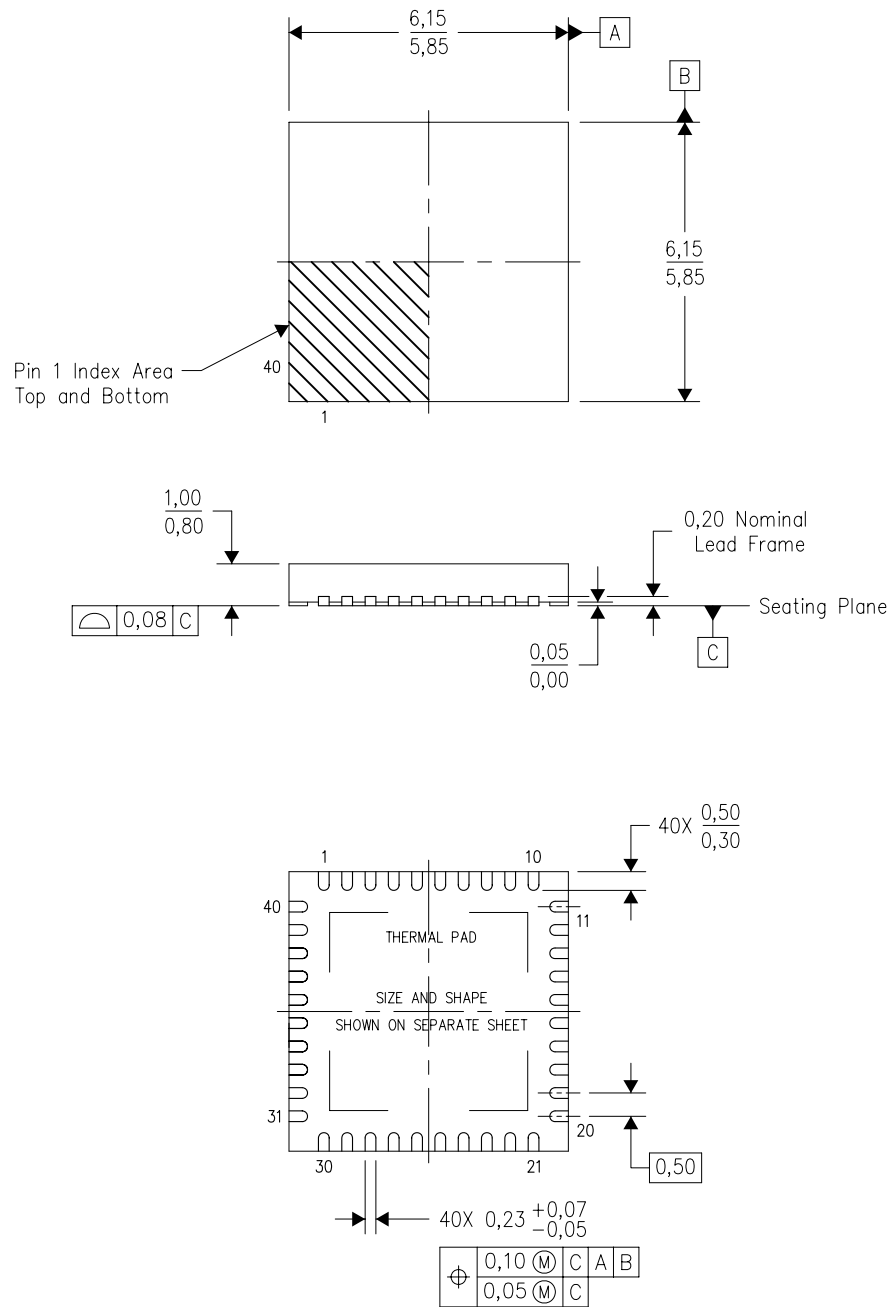
PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste.
  - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RHA (S-PVQFN-N40)

PLASTIC QUAD FLATPACK NO-LEAD



Bottom View

4204276/E 06/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - QFN (Quad Flatpack No-Lead) Package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Package complies to JEDEC MO-220 variation VJJD-2.



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